How Much Faster Can We Go? A Technology Outlook

Yusuf Leblebici
Swiss Federal Institute of Technology (EPFL)
Microelectronic Systems Laboratory

yusuf.leblebici@epfl.ch

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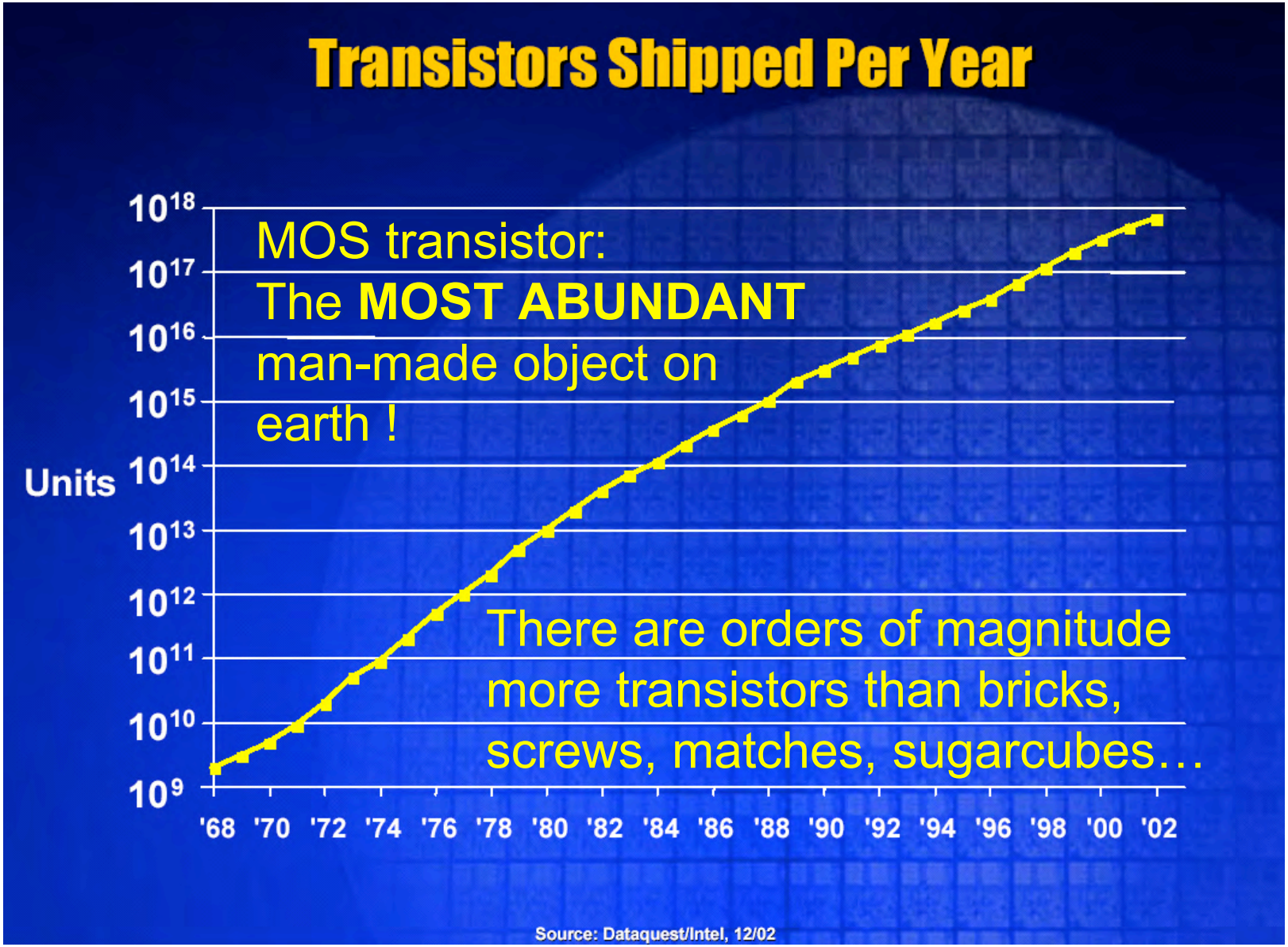
Acknowledgements

- Christof Paar
- Frank K. Gürkaynak
- Many colleagues at EPFL
- Entire LSM Team

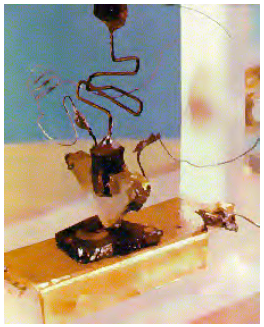
Outline

- Some history
- Current trends in large-scale integration
- Technology scaling and its future
- Nanodevices / nanoelectronics
- Architectural trends / outlook
- Potential problems down the road
- Fundamental limitations (?)
- Some future perspectives


Transistors Shipped Per Year
MOS transistor:
The MOST ABUNDANT
man-made object on
earth !
There are orders of magnitude
more transistors than bricks,
screws, matches, sugarcubes…
Units
10^18
10^17
10^16
10^15
10^14
10^13
10^12
10^11
10^10
10^9
'68 '70 '72 '74 '76 '78 '80 '82 '84 '86 '88 '90 '92 '94 '96 '98 '00 '02
Source: Dataquest/Intel, 12/02

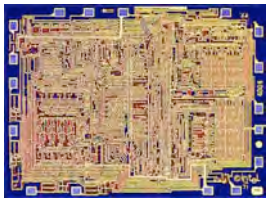
Some History

Invention of the transistor (BJT) 1947
Shockley, Bardeen, Brattain – Bell Labs

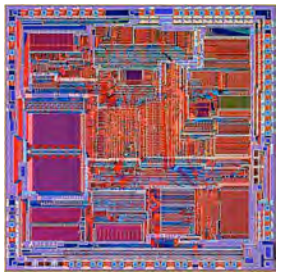


Single-transistor integrated circuit 1958
Jack Kilby – Texas Instruments

Invention of CMOS logic gates 1963
Wanlass & Sah – Fairchild Semiconductor



First microprocessor (Intel 4004) 1970
2,300 MOS transistors, 740 kHz clock frequency

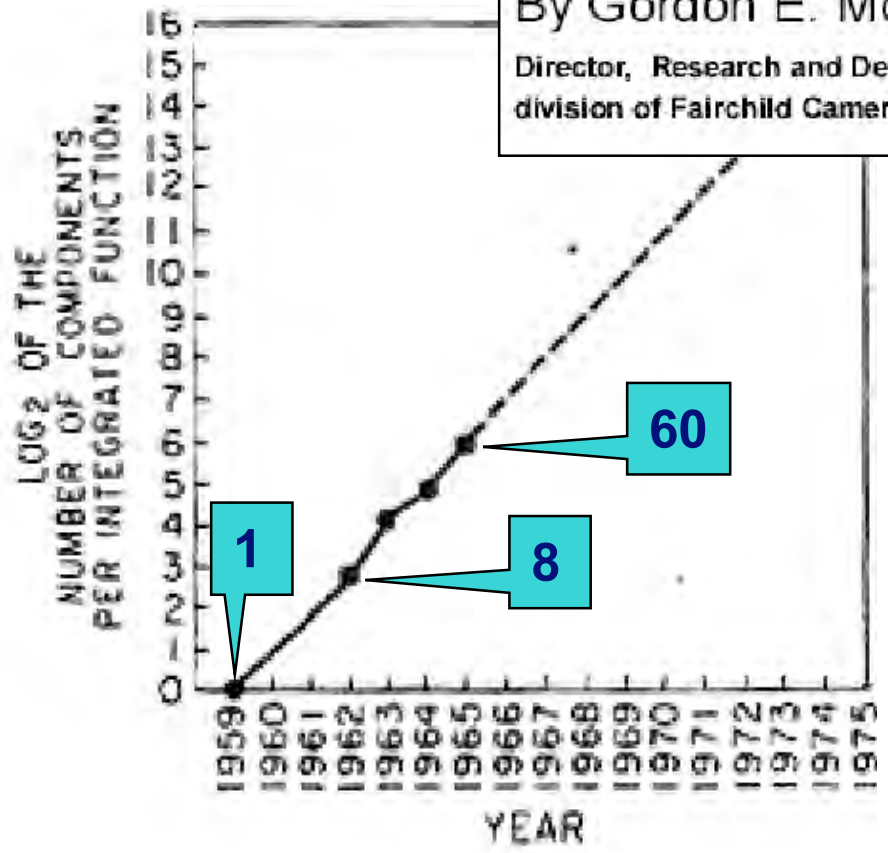


Very **L**arge **S**cale **I**ntegration 1978
Chips with more than ~20,000 devices

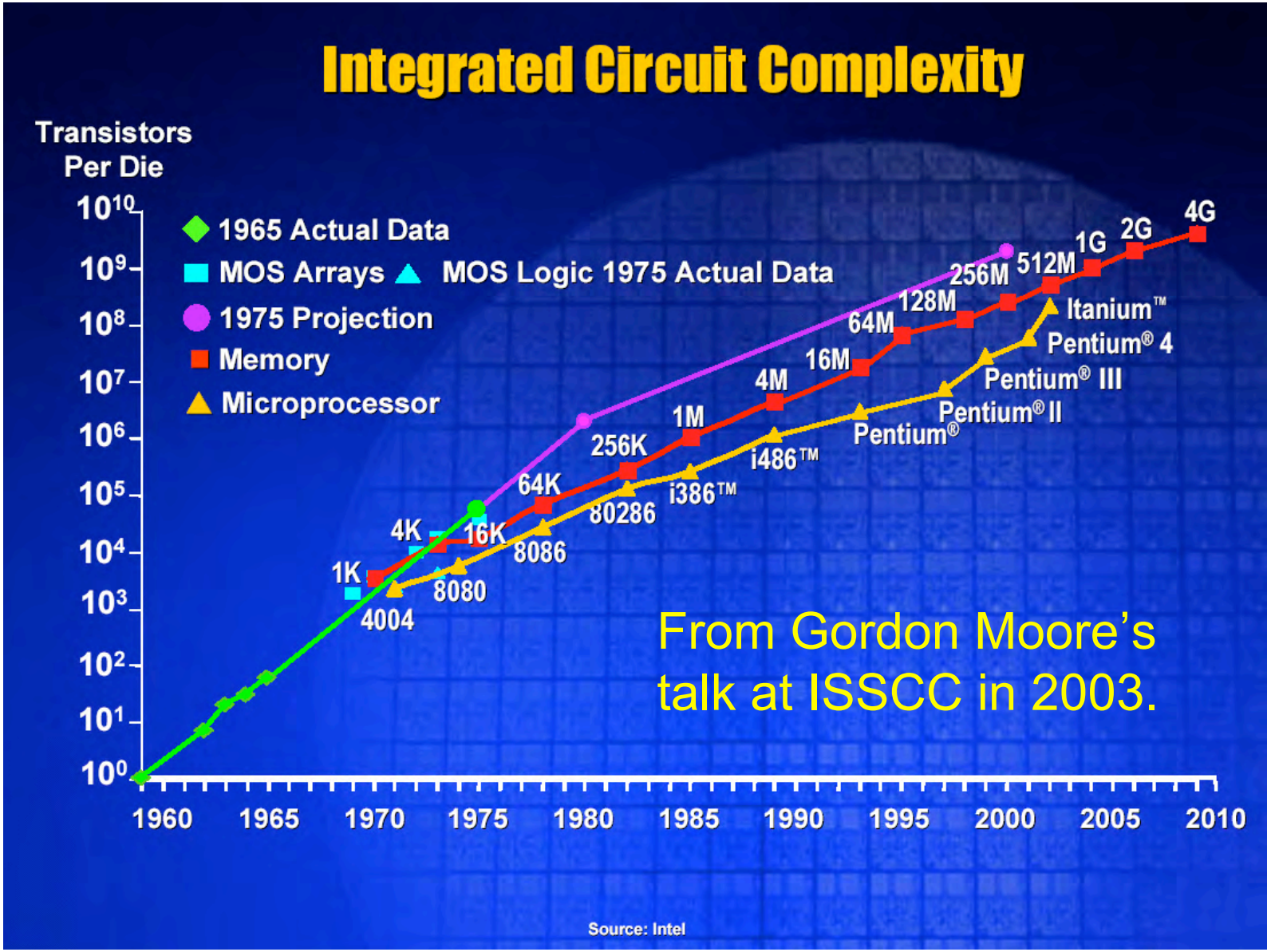
With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.



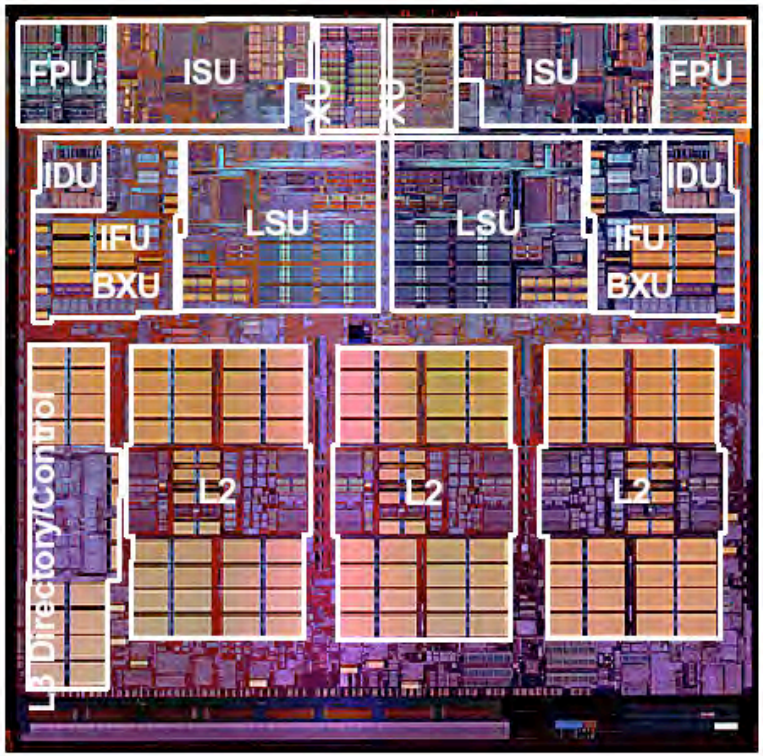
Prediction made in 1965, based on VERY limited data.


Integrated Circuit Complexity
Transistors Per Die
10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
10^{5}
10^{4}
10^{3}
10^{2}
10^{1}
10^{0}
1965 Actual Data
MOS Arrays
MOS Logic 1975 Actual Data
1975 Projection
Memory
Microprocessor
1K
4K
16K
64K
256K
1M
4M
16M
64M
128M
256M
512M
1G
2G
4G
4004
8080
8086
80286
i386™
i486™
Pentium®
Pentium® II
Pentium® III
Pentium® 4
Itanium™
1960
1965
1970
1975
1980
1985
1990
1995
2000
2005
2010
From Gordon Moore's talk at ISSCC in 2003.
Source: Intel

Some Leading-Edge Examples

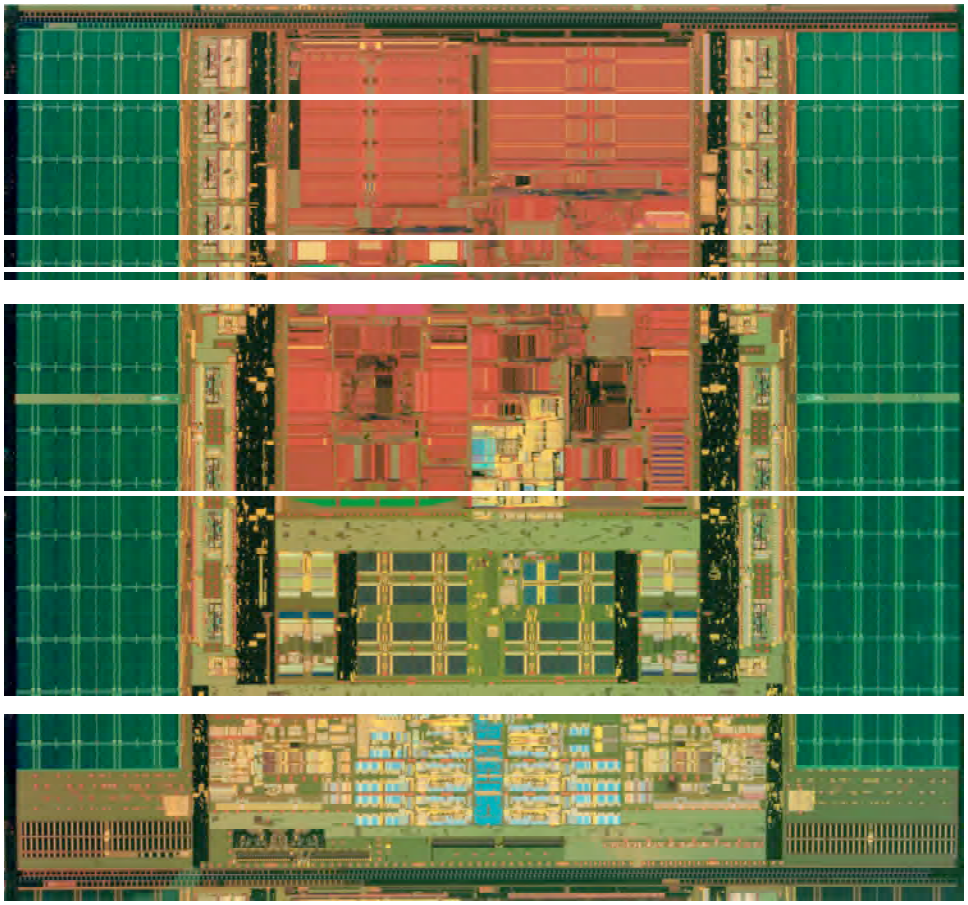
- >1 GHz frequency
- 174M transistors
- 0.18um lithography
  - Silicon on Insulator (SOI)
- 7 levels of metal
  - Copper interconnect
  - >1 mile of wire
- 4375 total macros
  - 430 unique custom macros
  - 50 unique SRAMs
  - 523 unique synthesized macros
  - ~100K buffers/inverters

Power dissipation 85 W !



IBM S4 processor (2001)

DEC Alpha 21364



- Introduced in 2003
- 0.13 um SOI CMOS
- 251 mm^2
- Clock: 1.5 GHz
- 64 bit architecture
- **Power >100 W** (!)
- VDD = 1.2 V

Don’t think that the highest-performance processors are always found in a computer !!

- Sony Playstation II
- Chip designed by Toshiba
- Introduced in 1998
- 10,500,000 transistors
- 238 mm^2
- Clock: 300 MHz
- 128 bit architecture
- 10 floating-point multiplier accumulators
- MPEG-2 decoder
- Multimedia processor

Sony Playstation 3 Specifications

CPU: Cell Processor PowerPC-base Core operating @3.2GHz

1 VMX vector unit per core

512KB L2 cache

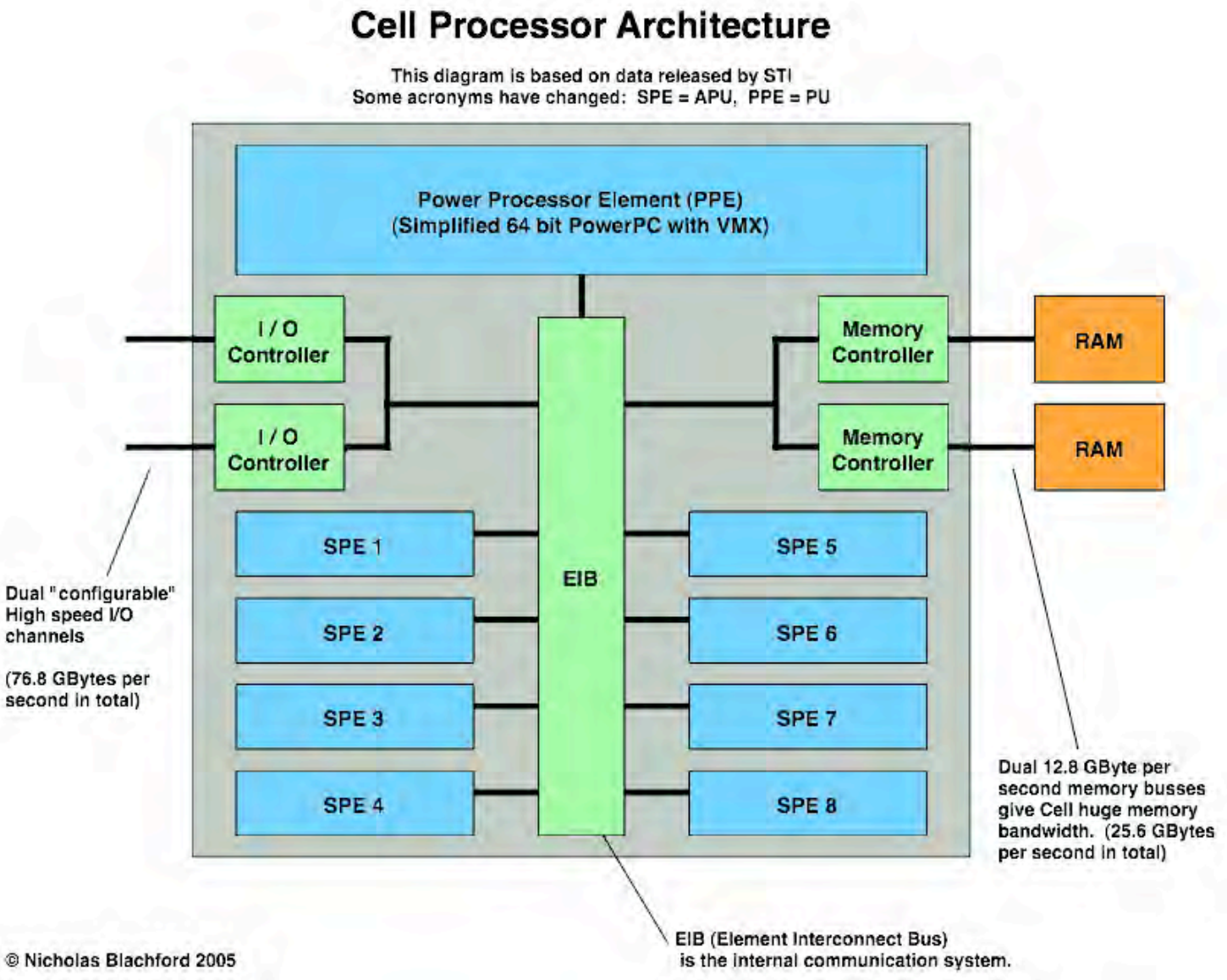
7 x SPE @3.2GHz

7 x 256KB SRAM for SPE

1 of 8 SPEs reserved for redundancy

Total floating point performance: **218 GIGAFLOPS**

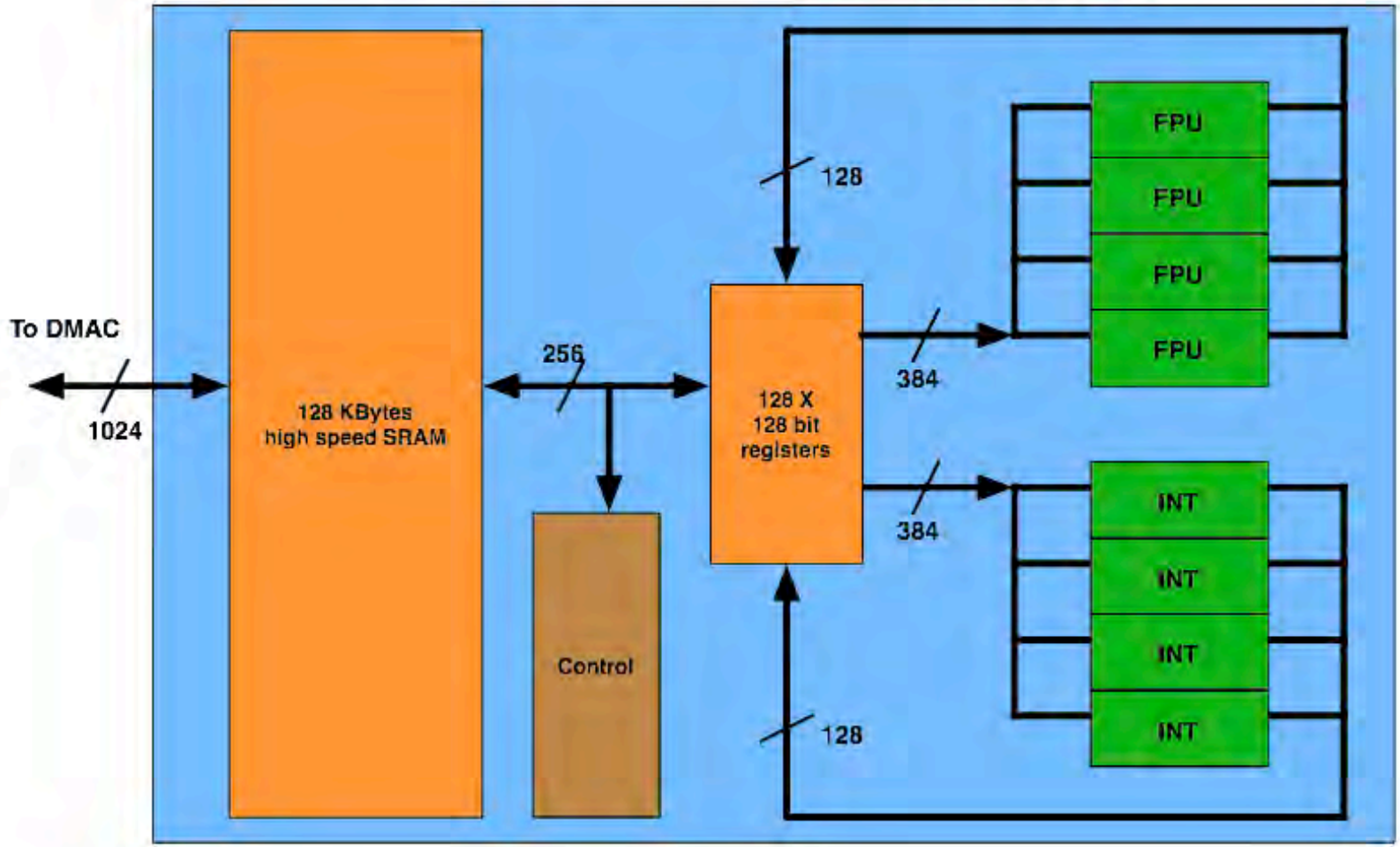
- STI (Sony, Toshiba, IBM) Cell
  - 9 Cores / 10 Execution threads
  - F = 4.6 GHz @ V = 1.3v
    - Covers 85% of die
  - P = 50 ~ 80W (estimated)
  - 512KB L2 Cache
  - Die Size: 221 mm^2
  - 234M Transistors
  - 90nm SOI technology (Low K, 8 layers, Cu interconnect)
  - 6.4GT/s I/O interface
  - 4 x 128 bit internal bus (ring)



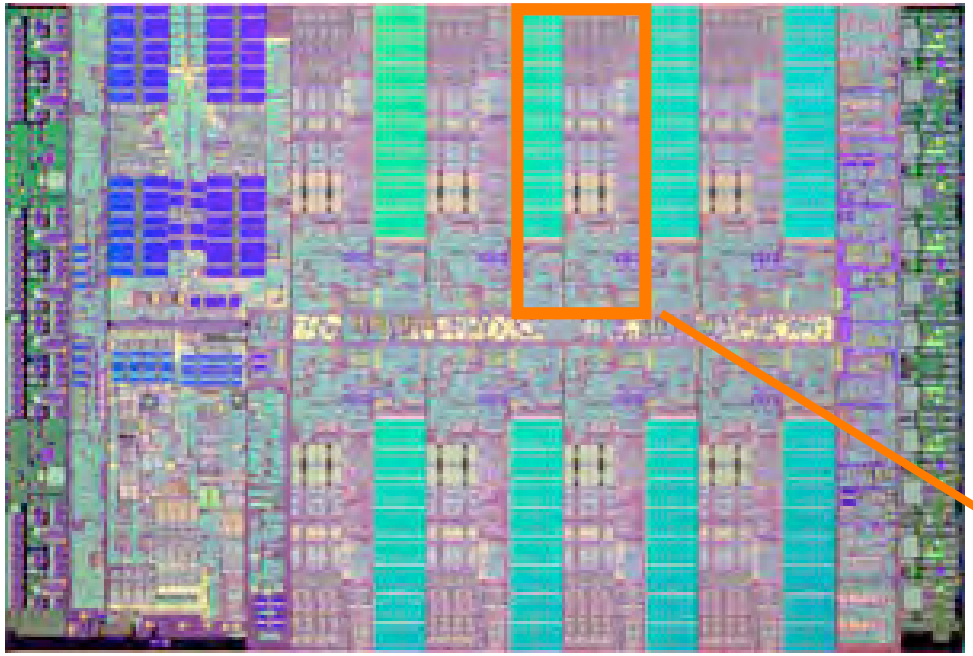
IBM / Sony / Toshiba Cell Processor

Cell APU Architecture

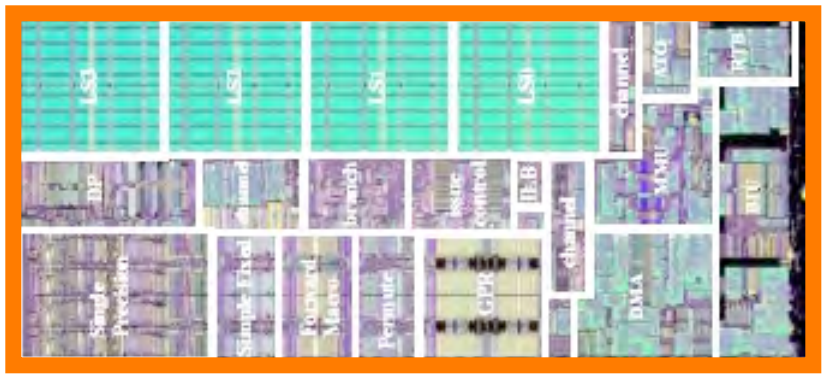
Each APU is an independent vector CPU capable of 32 GFLOPs or 32 GOPs.



© Nicholas Blachford 2005



IBM / Sony Cell Processor



Peak performance 256 GigaFlops

0.256 Tera Flops

World Fastest Supercomputer
IBM Blue Gene

70 Tera Flops !!

ITRS - International Technology Roadmap for Semiconductors (2005 Edition)

YEAR	2004	2007	2010	2013	2016
TECHNOLOGY	90 nm	65 nm	45 nm	32 nm	22 nm
CHIP SIZE	550 mm^2	550 mm^2	550 mm^2	550 mm^2	550 mm^2
NUMBER OF TRANSISTORS (LOGIC)	553 M	1 Billion	2 Billion	4.5 Billion	8.5 Billion
DRAM CAPACITY	1.0 Gbits	2.0 Gbits	4.3 Gbits	8.5 Gbits	35 Gbits
MAXIMUM CLOCK FREQUENCY	4.1 GHz	9.3 GHz	15 GHz	23 GHz	40 GHz
MINIMUM SUPPLY VOLTAGE	0.9 V	0.8 V	0.7 V	0.6 V	0.5 V
MAXIMUM POWER DISSIPATION	150 W	190 W	200 W	200 W	200 W
MAXIMUM NUMBER OF I/O PINS	3000	4000	4000	5300	7000

Predictions of the worldwide semiconductor / IC industry about its own future prospects...

ITRS - International Technology Roadmap for Semiconductors (2005 Edition)

Shrinking Device Dimensions

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Increasing Function Density

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DRAM CAPACITY	**1 Gbits**	**2 Gbits**	**4 Gbits**	**9 Gbits**	**35 Gbits**
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Increasing Clock Frequency

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Decreasing Supply Voltage / Increasing Power

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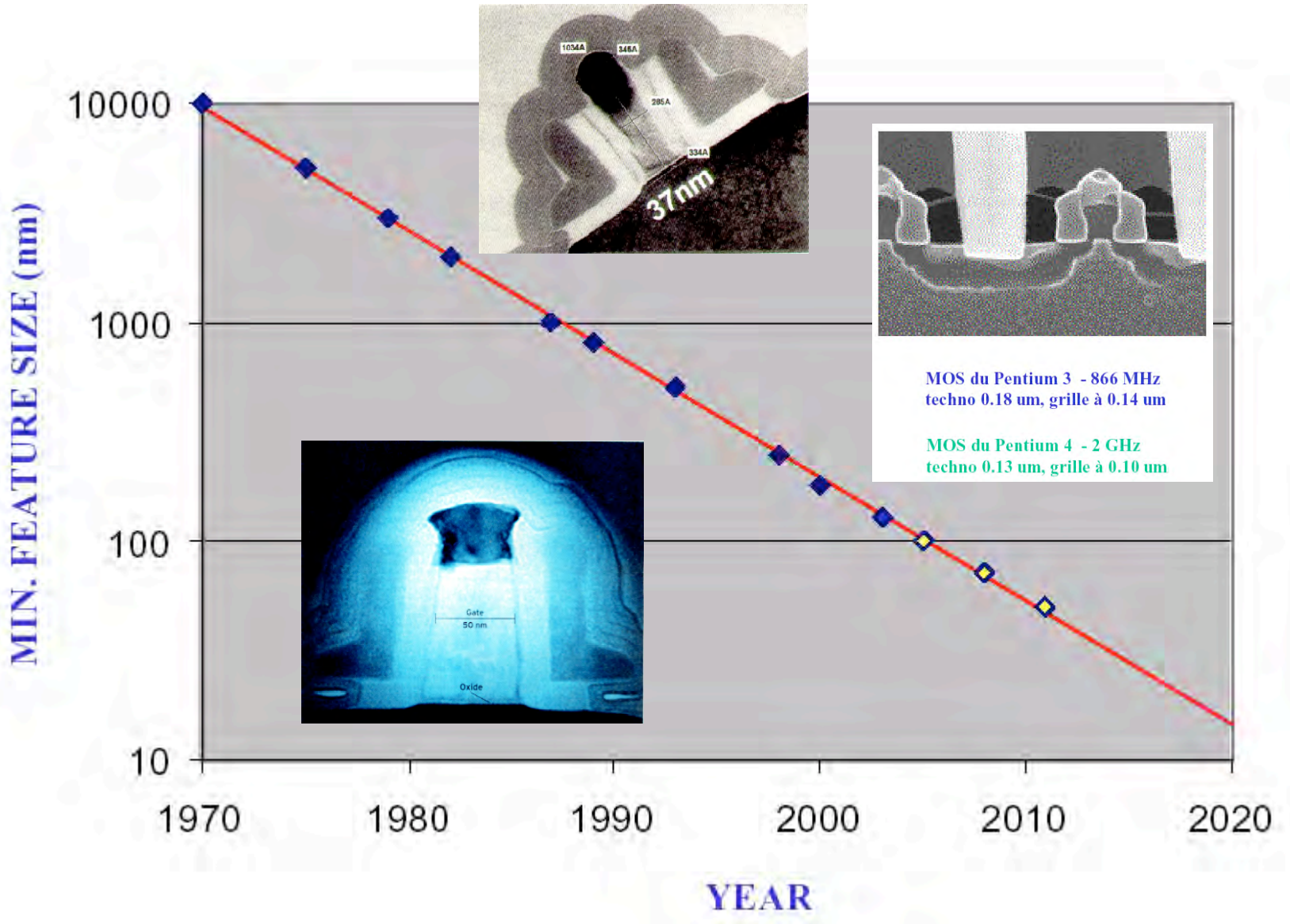
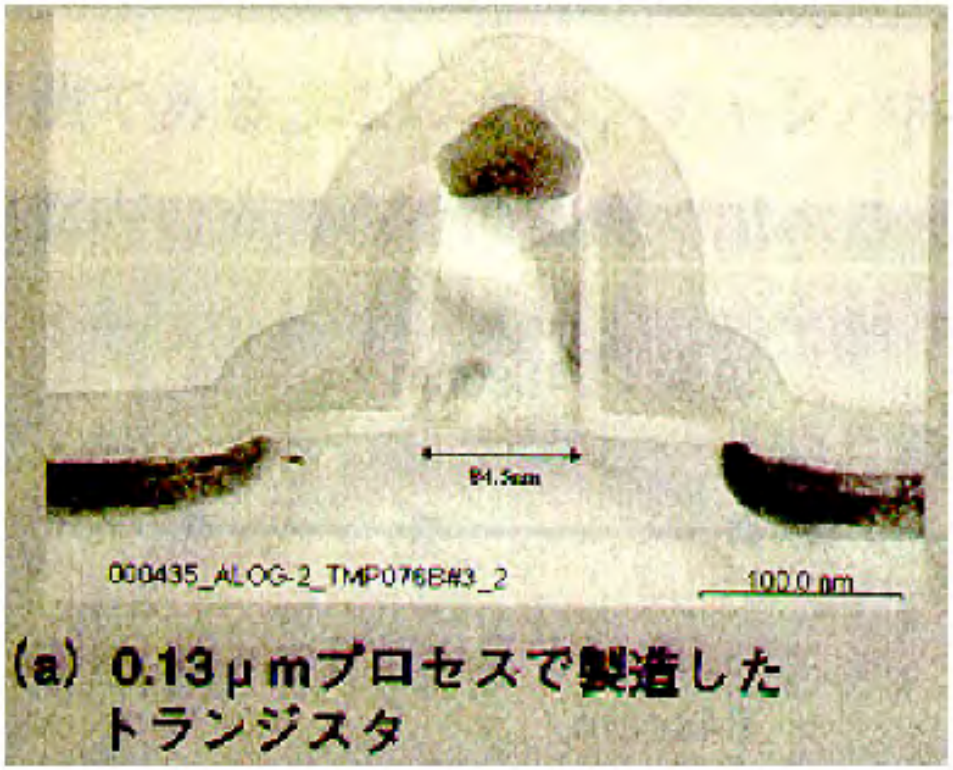

MIN. FEATURE SIZE (nm)
10000
1000
100
10
1970
1980
1990
2000
2010
2020
YEAR
1034A
346A
285A
334A
37nm
Gate
50 nm
Oxide
MOS du Pentium 3 - 866 MHz
techno 0.18 um, grille à 0.14 um
MOS du Pentium 4 - 2 GHz
techno 0.13 um, grille à 0.10 um

What Do These Transistors Look Like ?

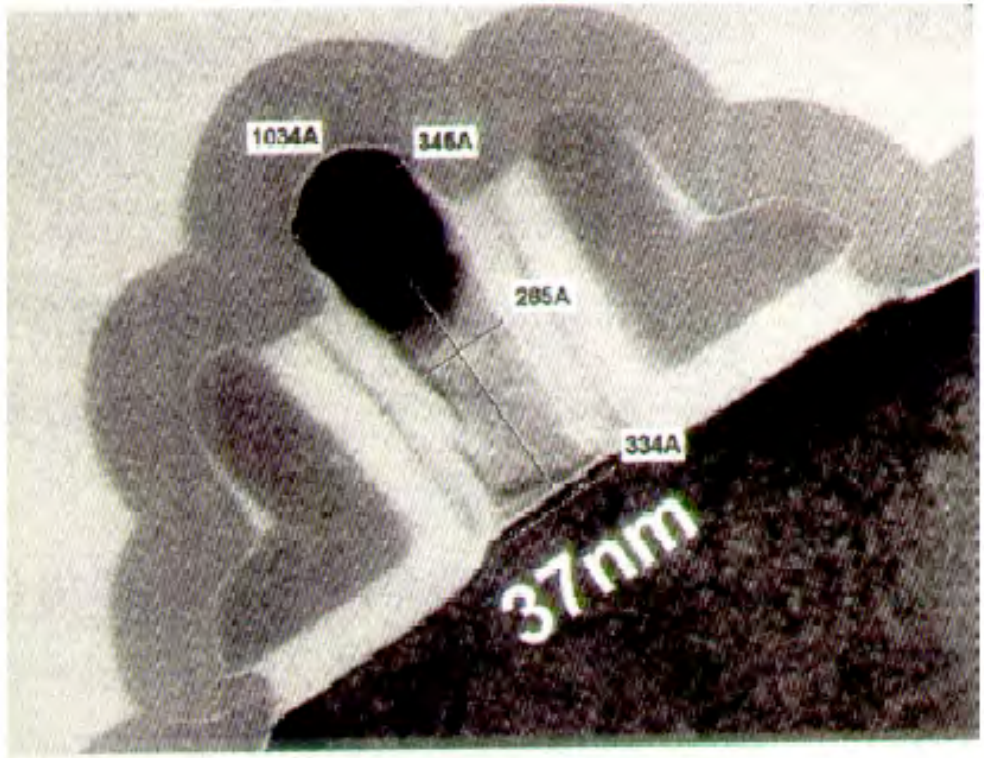


TSMC
0.13μ

Source:
Nikkei
Microdevices
11/00

What Do These Transistors Look Like ?

TI
0.09µ



(a) 90nmノード向けトランジスタ

Source: Nikkei Microdevices 9/02

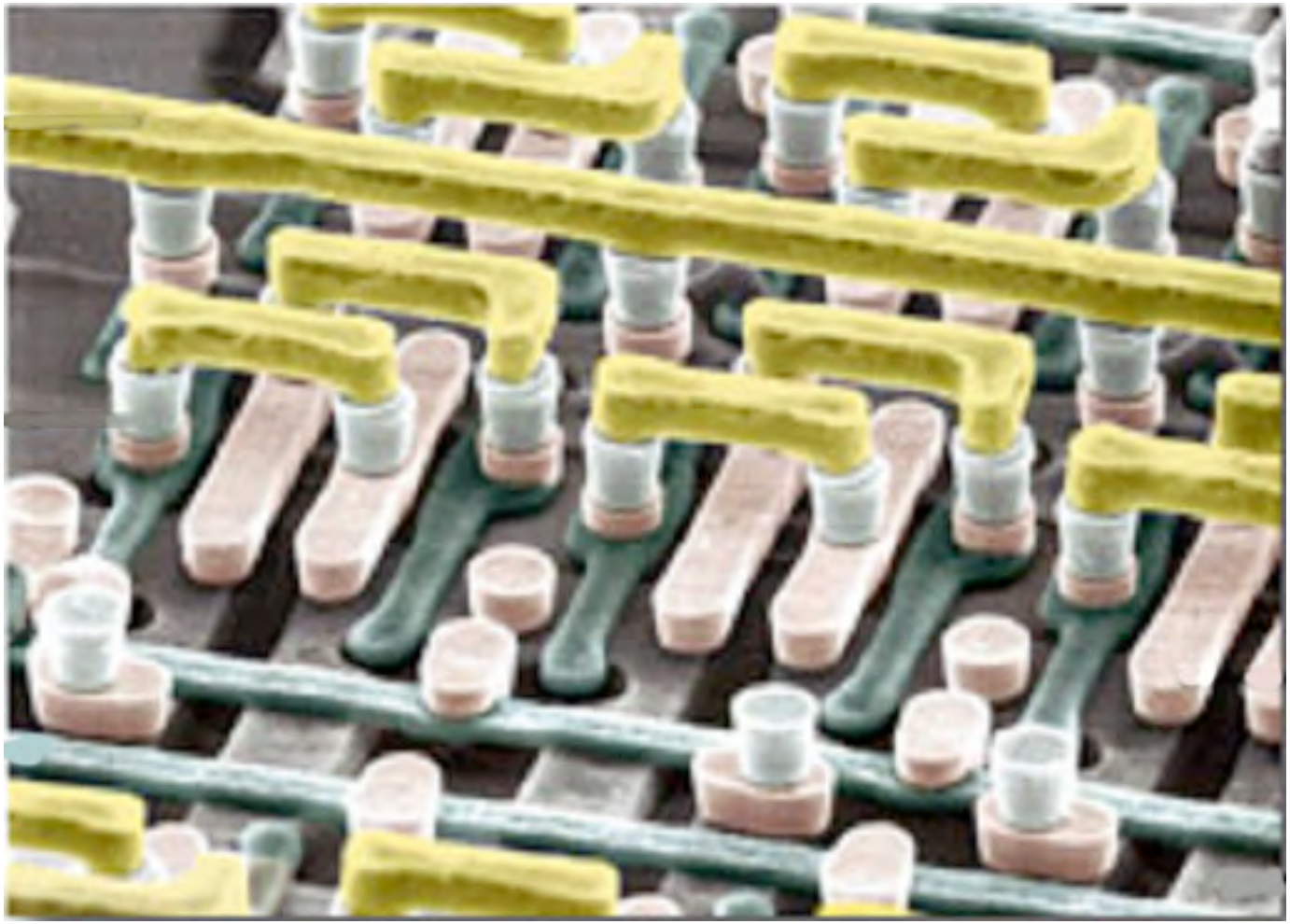
Multi-Level Metal Interconnect

TSMC
0.13μ
8 layers
Cu

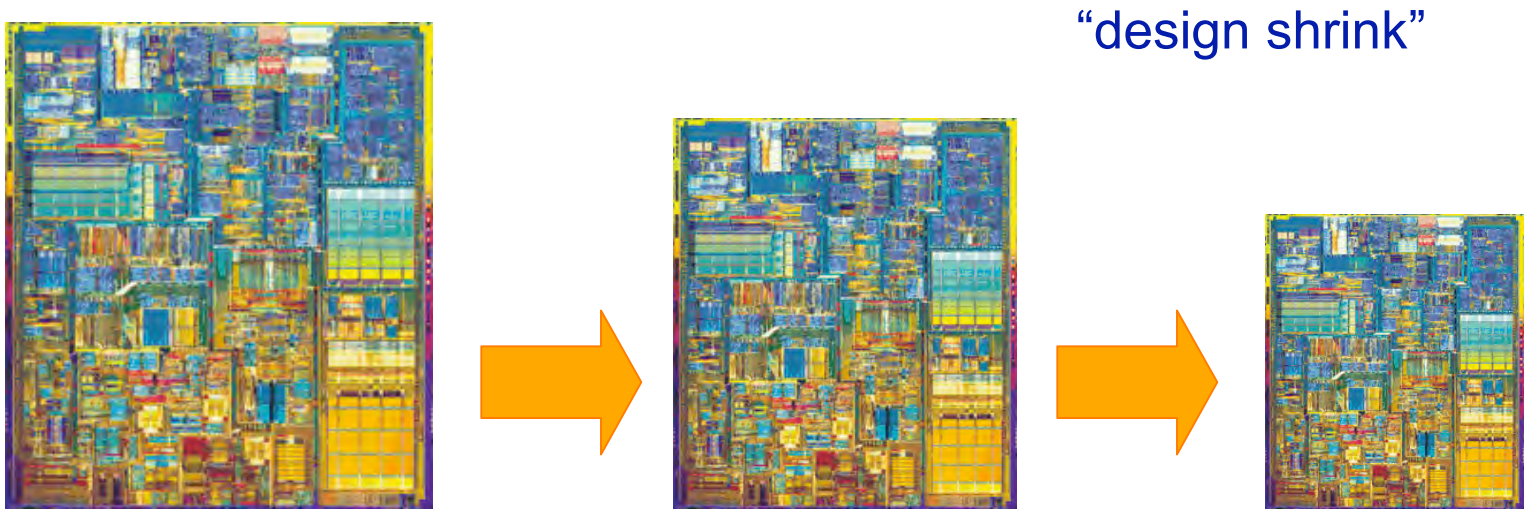
Source:
Nikkei
Microdevices
11/00

Multi-Level Metal Interconnect

Multi-Level Metal Interconnect



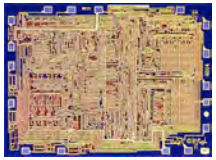
Lithography Resolution is Decreasing



With each new technology generation, we would be able to fit the same amount of functionality into a **smaller** silicon area (ideally).

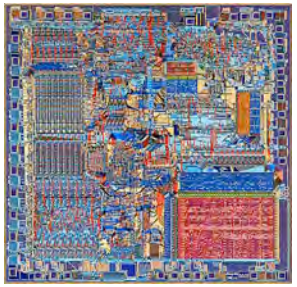
Lithography Resolution is Decreasing

1971



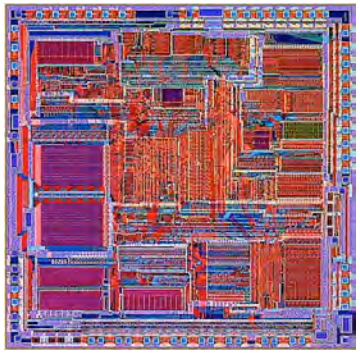
10 μm technology
12 sqmm

1979



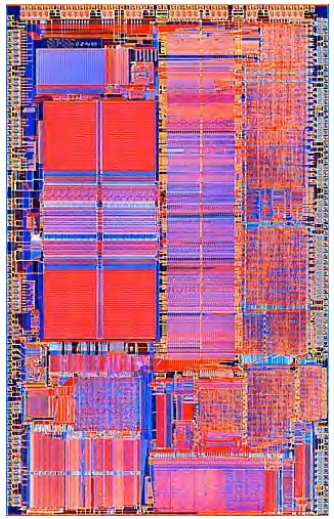
3 μm technology
33 sqmm

1982



1.5 μm technology
50 sqmm

1989

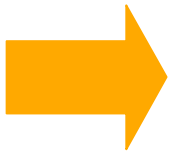


0.8 μm technology
81 sqmm

But at the same time, we try to put **more** functionality in each chip for each new technology generation, so that the average chip size actually **increases** over the years !

A Few Words on Clock Speed

Increasing Clock Frequency



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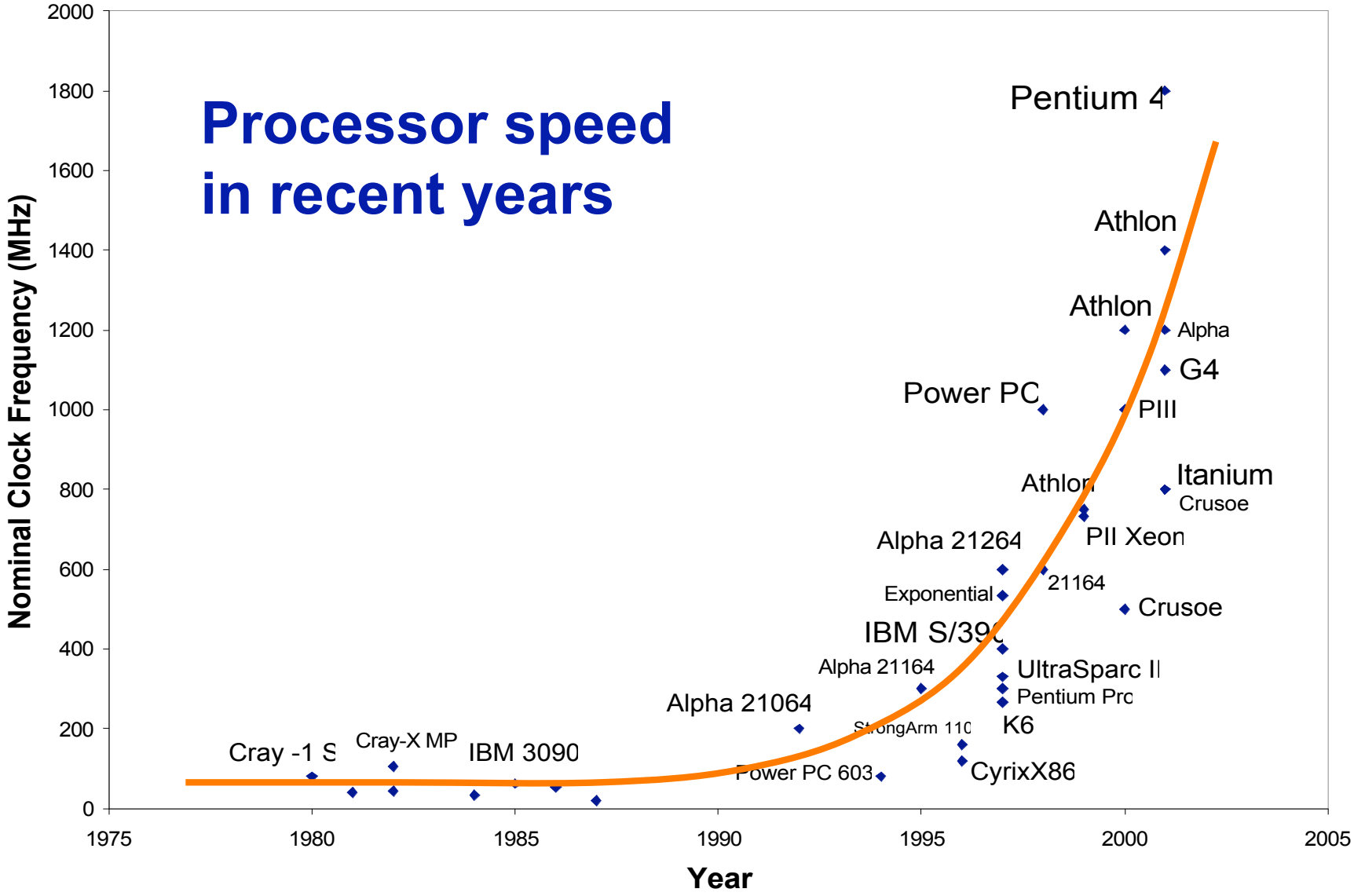
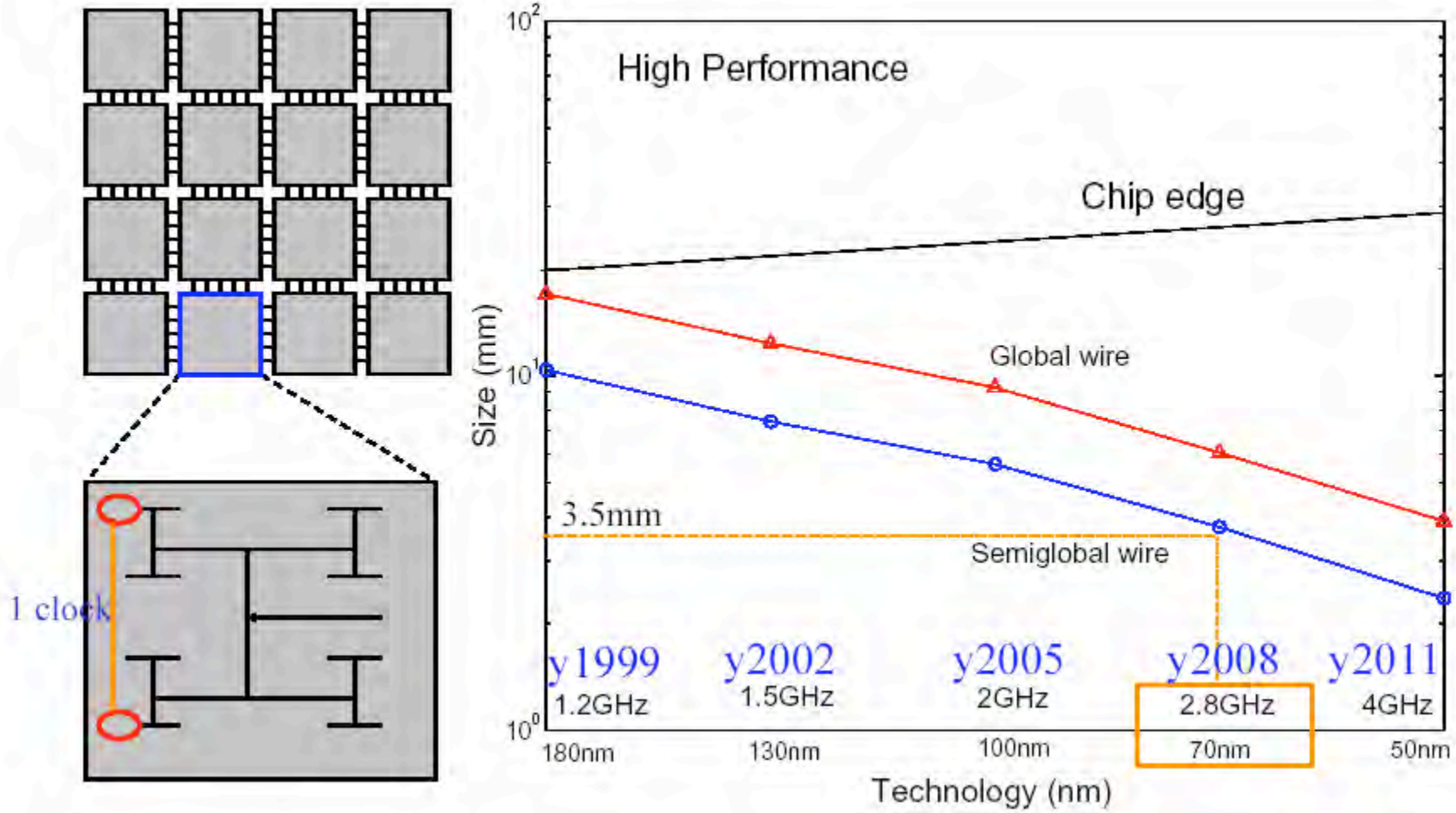
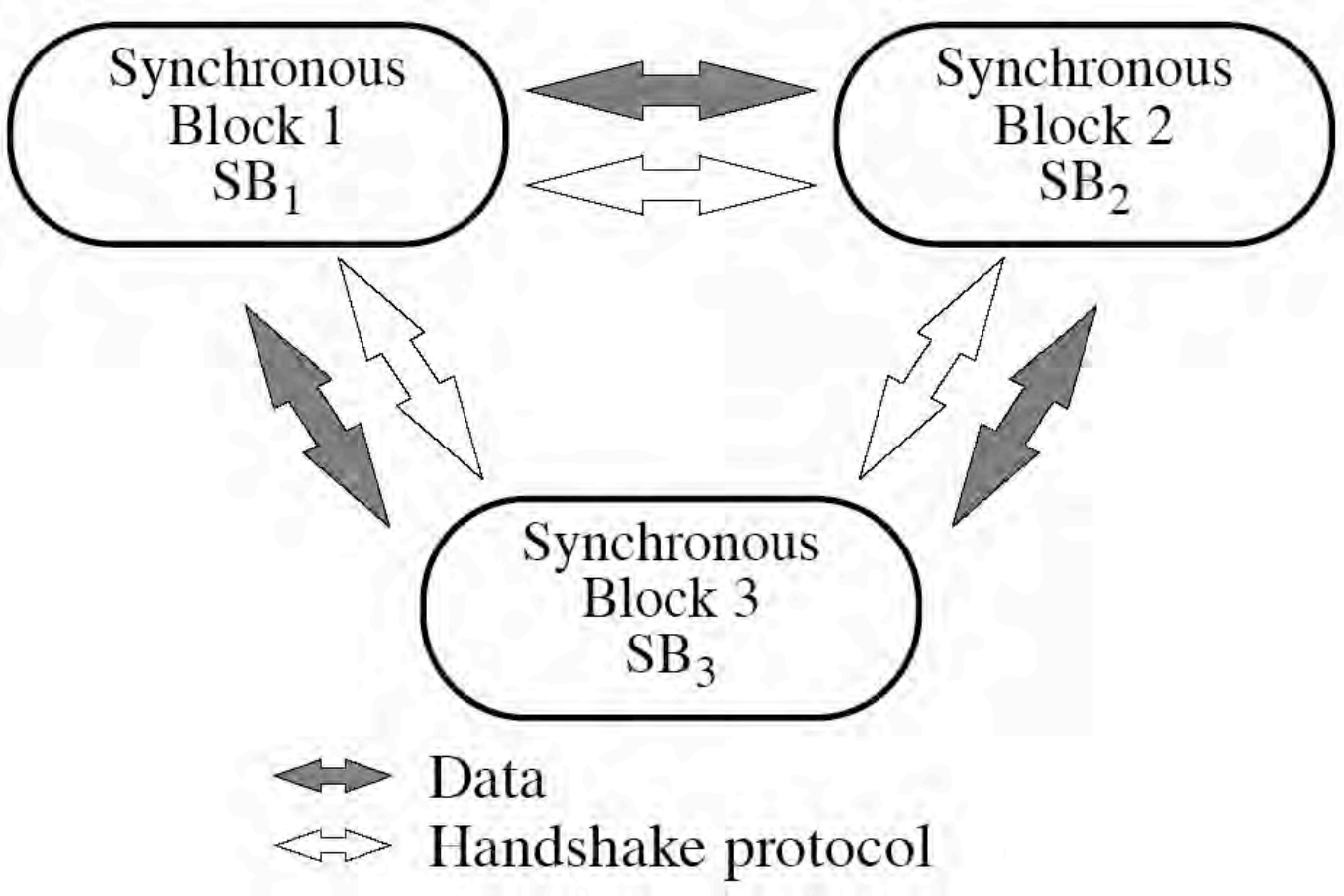
Processor speed in recent years



Entire Chip is Not Reachable in One Clock Cycle !

Entire Chip is Not Reachable in One Clock Cycle !





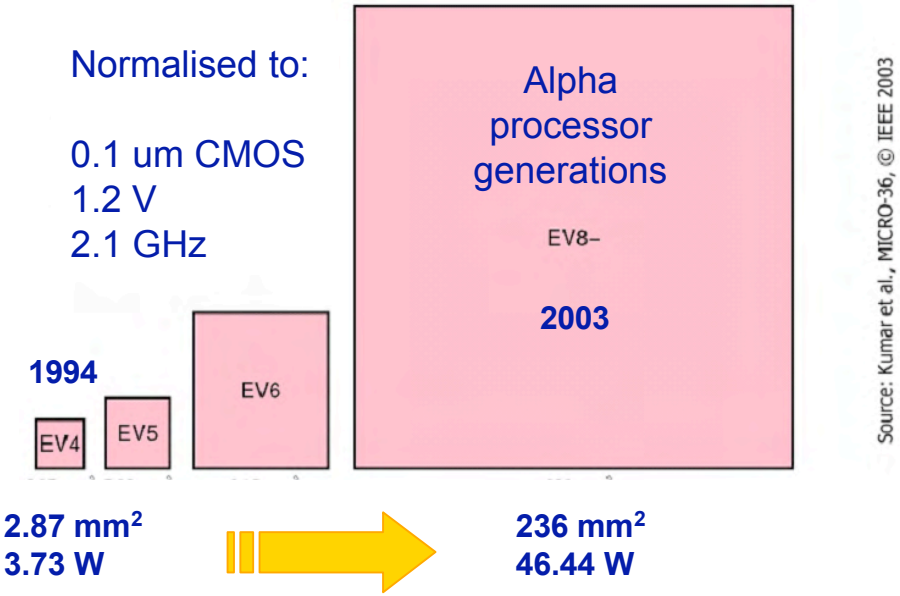
Globally asynchronous – locally synchronous (GALS) system

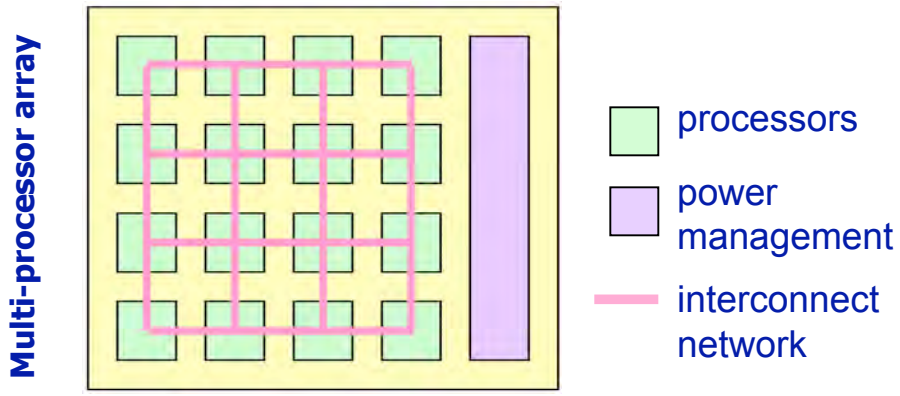
Single-Processor Systems Reach Their Limit

At constant technology:

- Area has increased by 80x
- Power has increased by 12x
- Performance has increased by 3x (!)

Area and power costs not affordable for mobile applications…

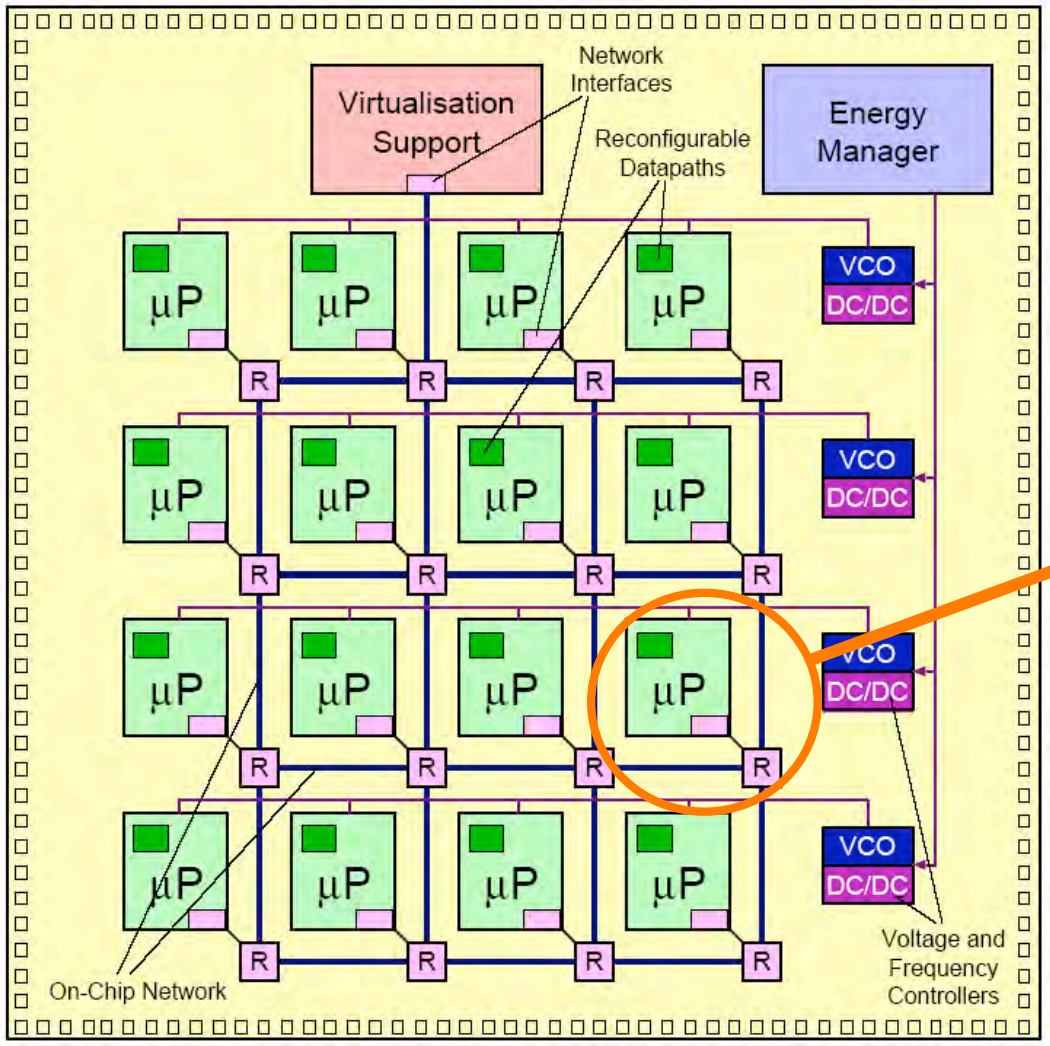


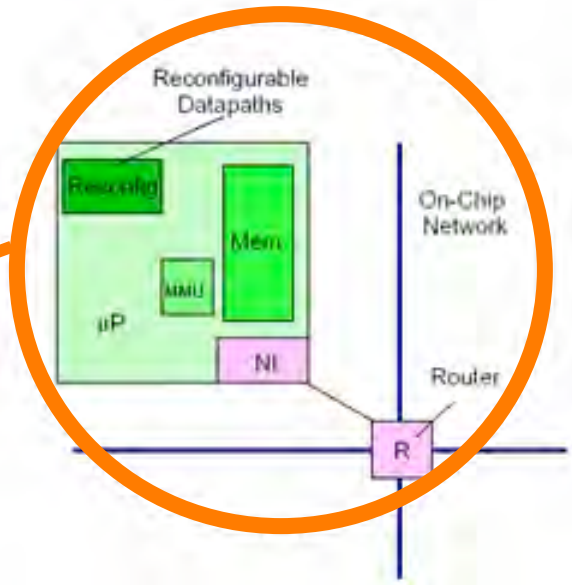


Possible solution:

Flexible multi-processor platform made up of a **large** number of **simple** embedded processors and a scalable Network-on-Chip (NoC) communication architecture.

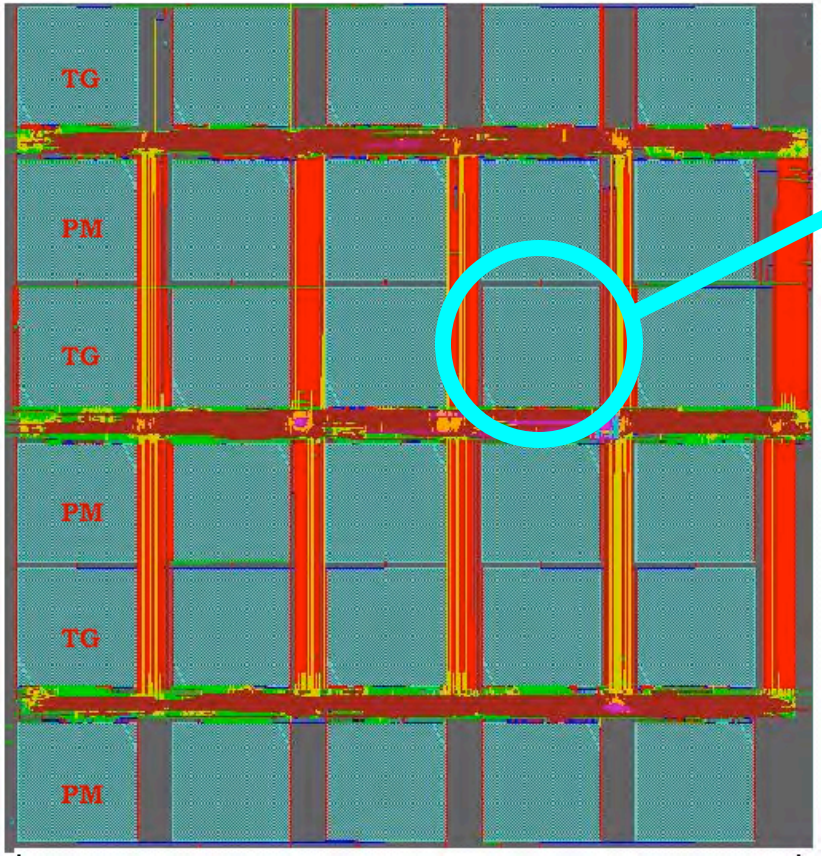
Many-Processor Platforms





Instead of "Multi-Processors"…

Many-Processor Systems

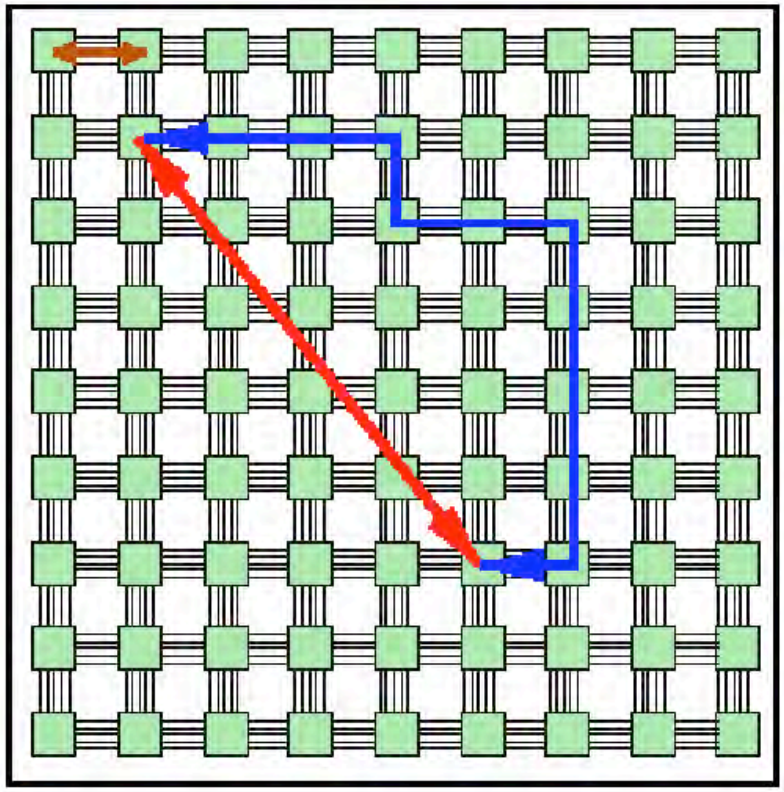


IP cores:
1 mm x 1 mm each

30 cores: 7.20 mm x 6.88 mm
Floorplan area: 49.5 sqmm

After Luca Benini, MPSoC 2005

Still: Massive Interconnect Requirements for Many-Processor Systems



Global interconnect demand for a 10x10 processor array:

37.5 km of wiring for P2P connections

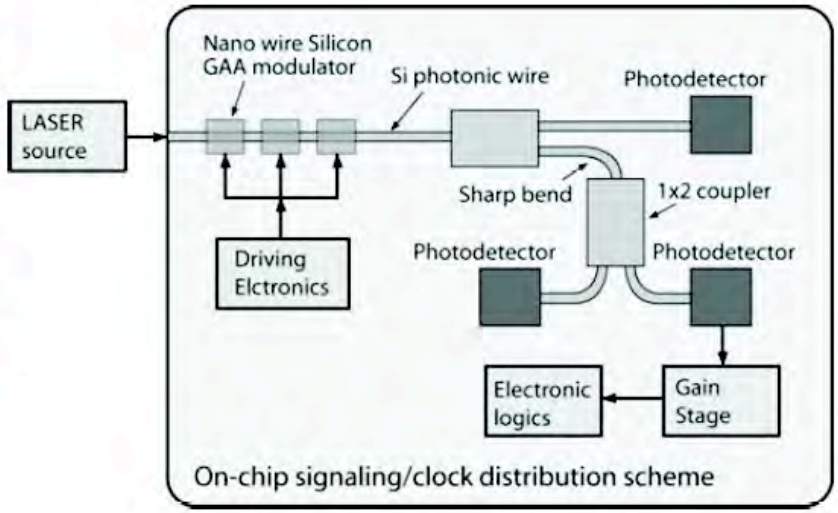
After Hannu Tenhunen, MPSoC 2005

Optical Interconnects ?

On chip guided wave optical clock distribution

Potentials

- Inherently synchronous for wafer-scale dimensions.
- Design does not need to be reconsidered for a change in modulation frequency.
- Immune to electromagnetic interference with adjacent electronics or RF signals.
- WDM and TDM are possible.



Limitations

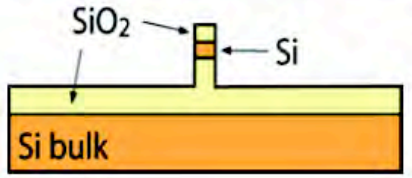
- Difficult to implement light sources, waveguide and detectors in the same substrate?
- High propagation and coupling loss.
- Challenges with regards to layout and process development.
- Dispersion may become relevant for long waveguides.
- Power still an issue, especially for short links (receiver dominated).

Components for on-chip optical signaling

Waveguiding

- Low propagation losses (<1dB/cm).
- Low bending losses and small band radii
  - Small waveguides with high *Dh*.
- Compact and low loss coupling devices.
- Waveguide dimension compatible with electronics size scale.

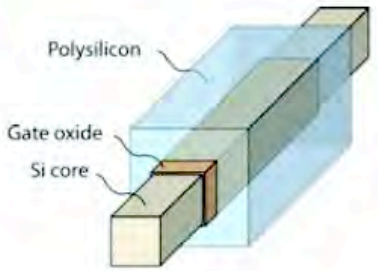
SOI photonic wire



Detection

- Monolithically integrated.
- Small size and low power.
- High efficiency.
- High speed.

SiGe detector



Clock source

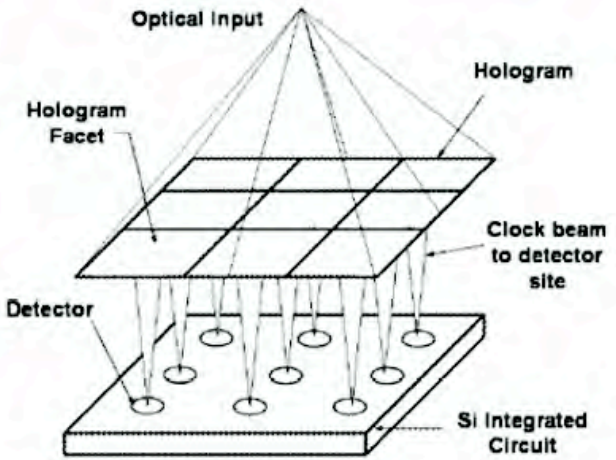
- External: Low loss, high efficiency coupling (mode size converter or grating).
- Internal: Monolithically or hybrid light source and GHz rate modulator.

External laser + modulator

On chip clock distribution

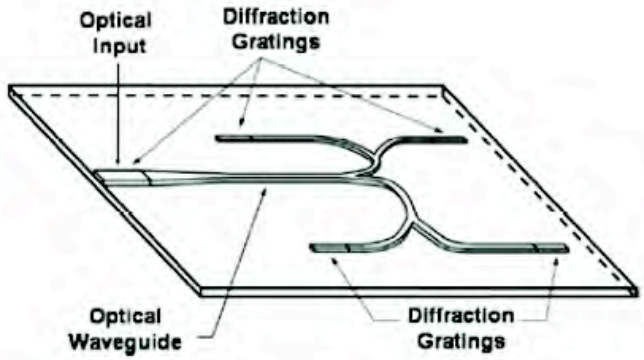
Free space

- External light source broadcasted to different photodetectors.
- Issues:
  - Holographic element required.
  - Photogeneration outside PD area.
  - Complicated, bulky(3D) and fragile.

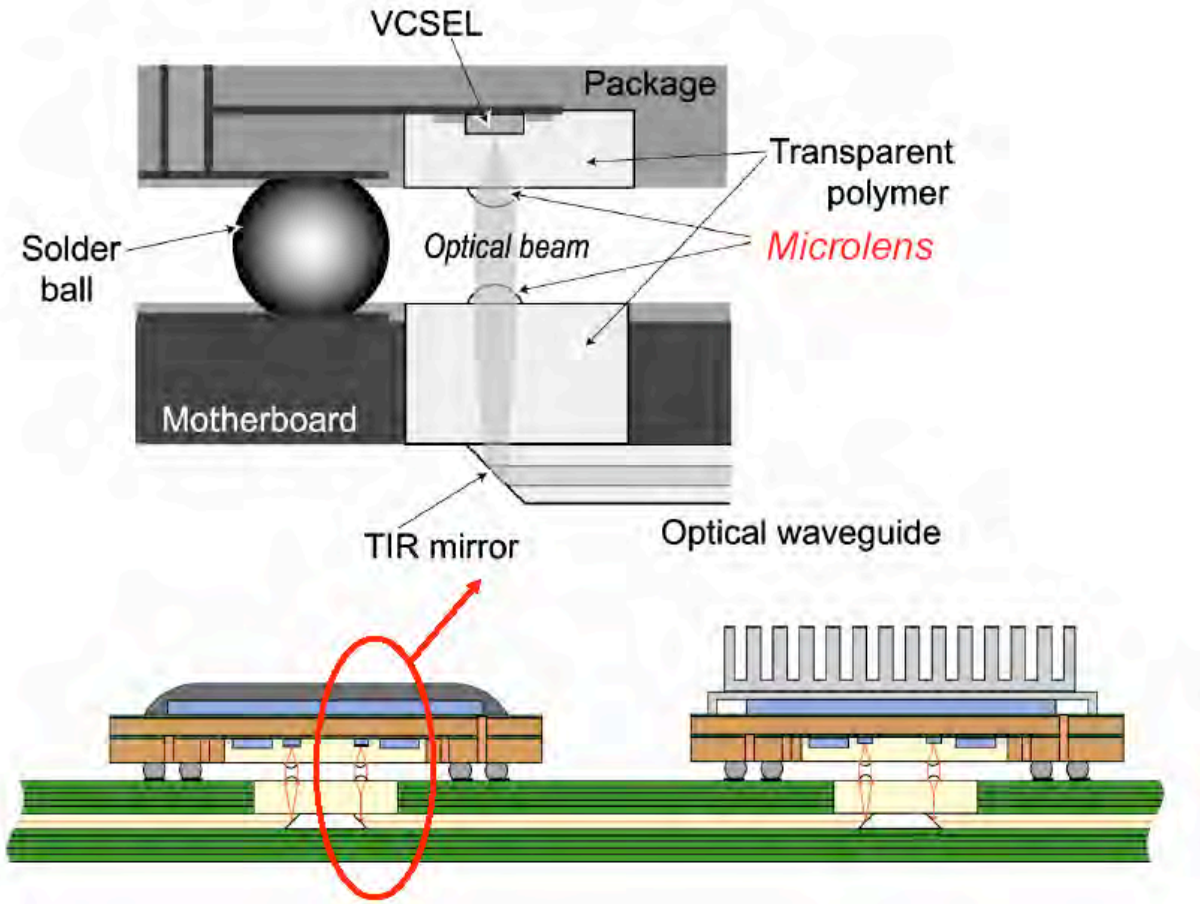


Guided wave

- External or internal light sources.
- Issues:
  - Propagation losses.
  - Bend losses.



Next-Generation Chip-to-Chip Links

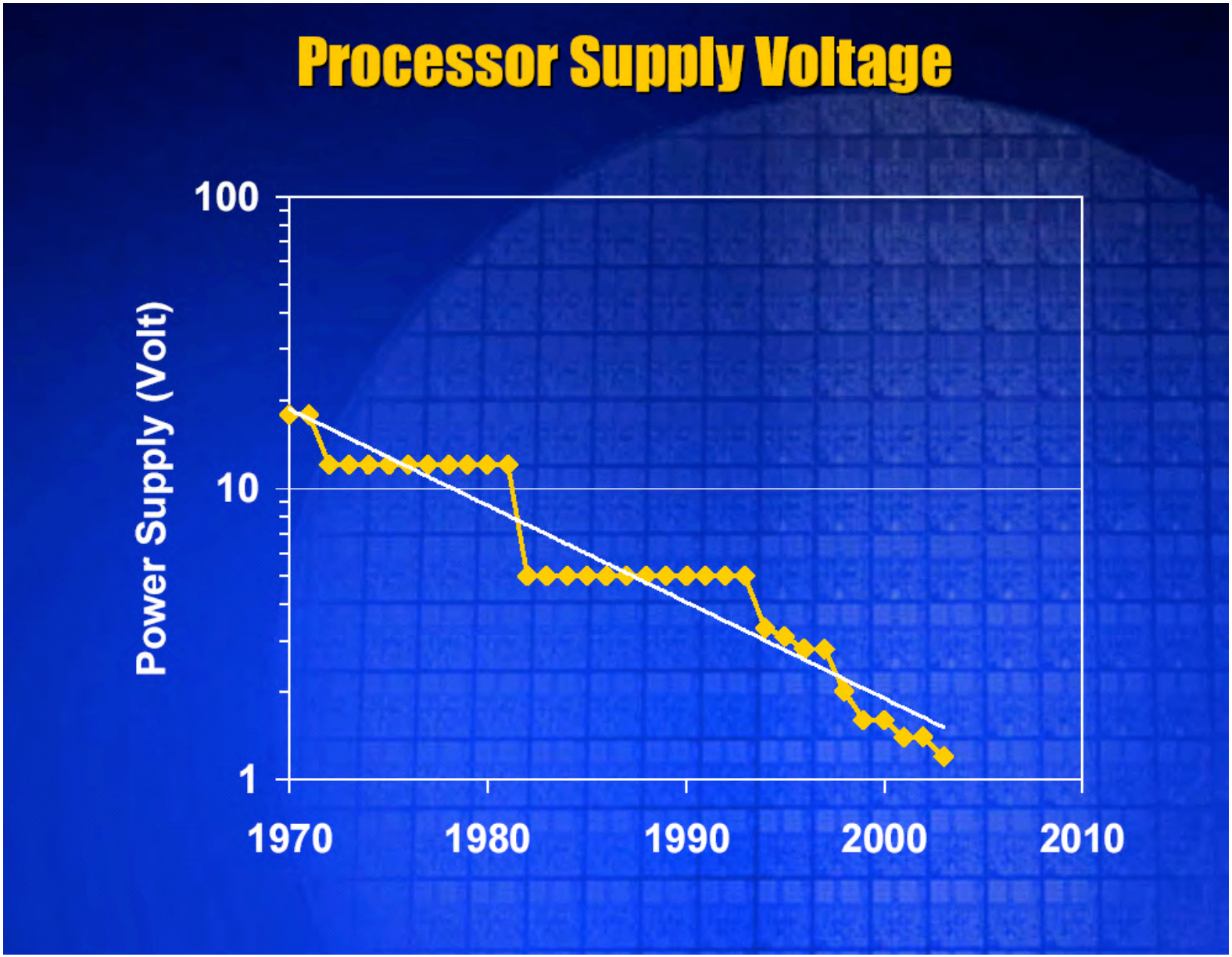


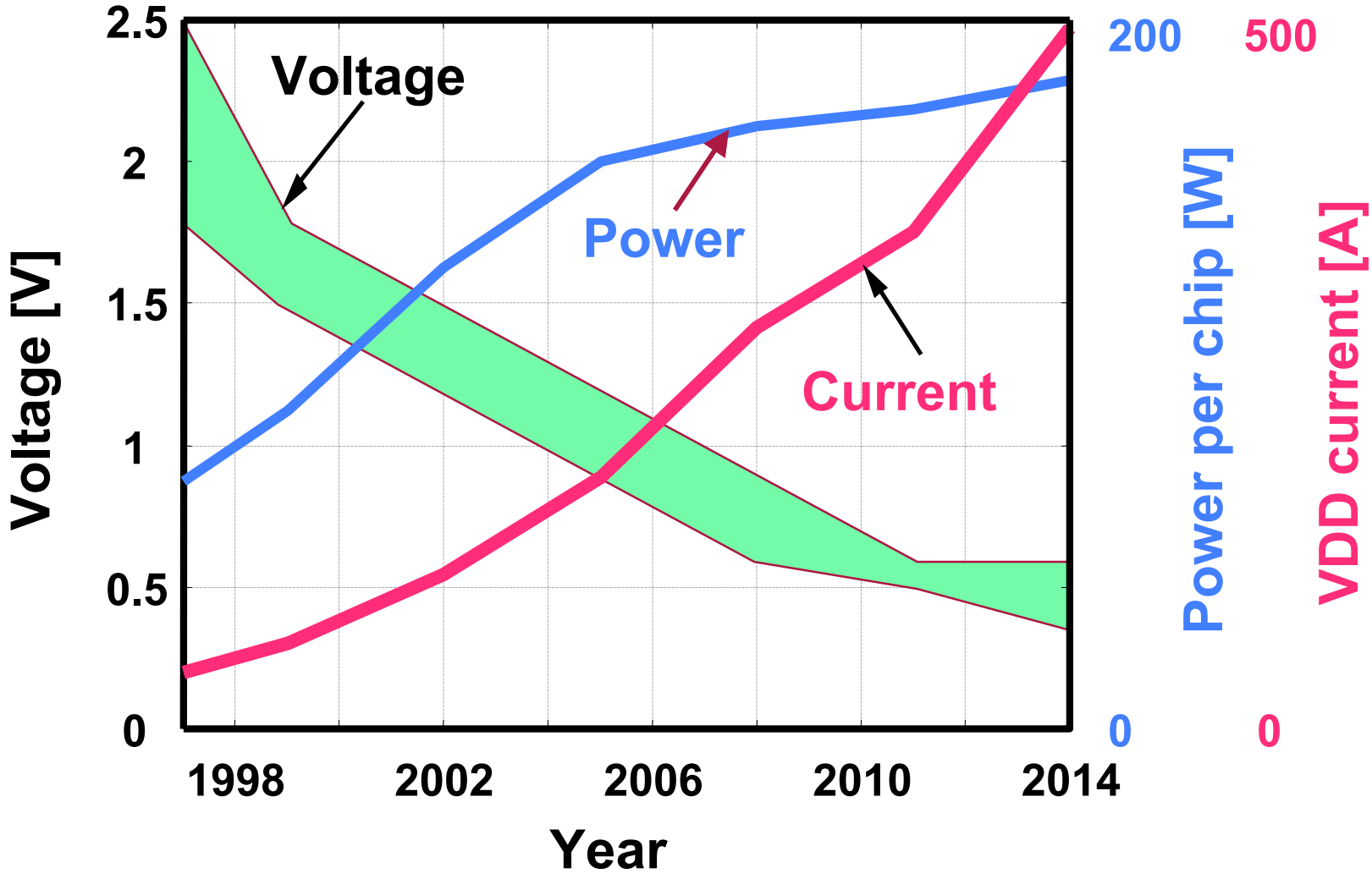
H.Takahara, Optoelectronic Packaging Trends in Japan , *Stanford University, US-Asia TMC, May 2003*

power, power, power…

Decreasing Supply Voltage / Increasing Power

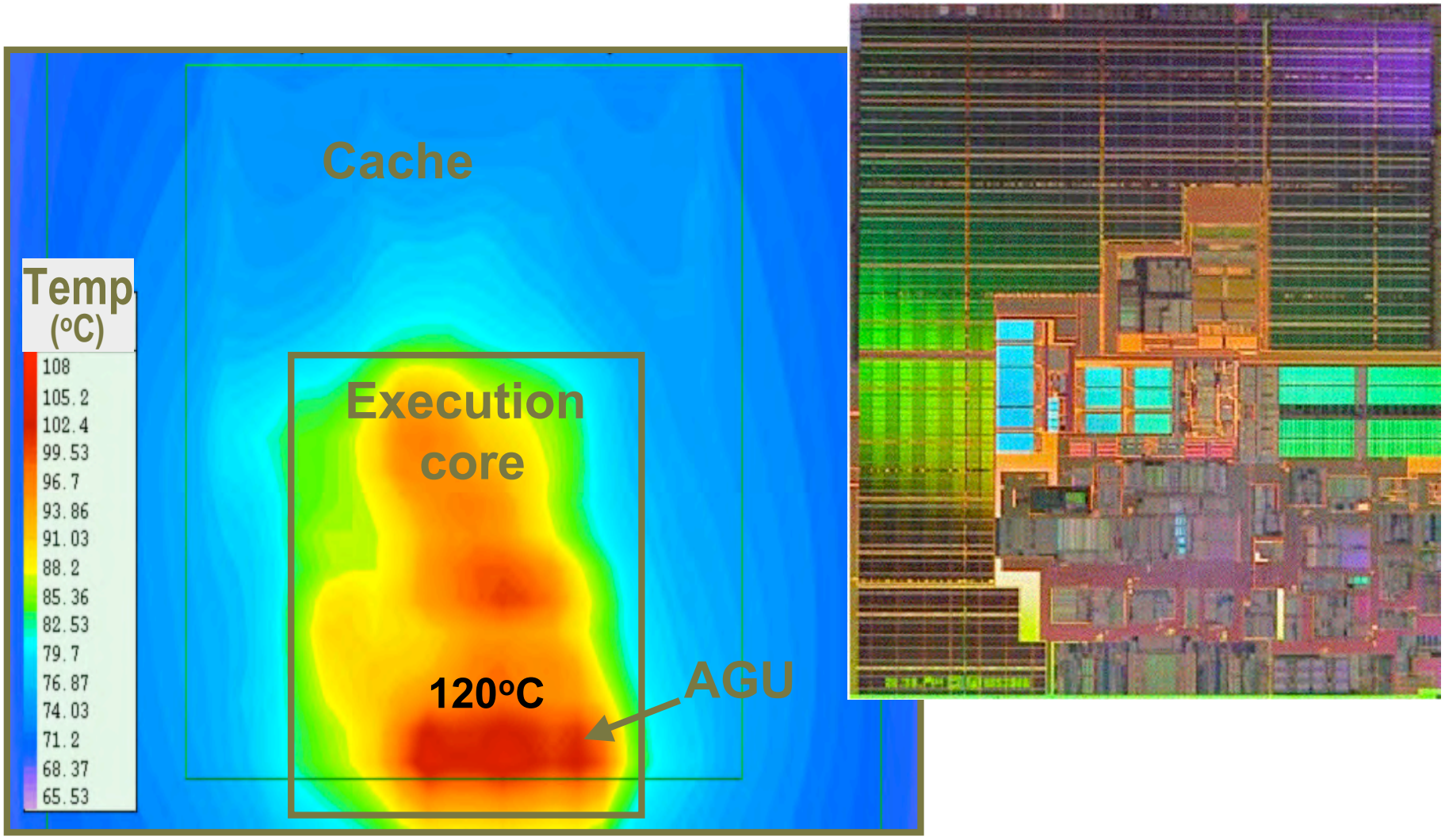
YEAR	2004	2007	2010	2013	2016
TECHNOLOGY	90 nm	65 nm	45 nm	32 nm	22 nm
CHIP SIZE	550 mm^2	550 mm^2	550 mm^2	550 mm^2	550 mm^2
NUMBER OF TRANSISTORS (LOGIC)	553 M	1 Billion	2 Billion	4.5 Billion	8.5 Billion
DRAM CAPACITY	1.0 Gbits	2.0 Gbits	4.3 Gbits	8.5 Gbits	35 Gbits
MAXIMUM CLOCK FREQUENCY	4.1 GHz	9.3 GHz	15 GHz	23 GHz	40 GHz
MINIMUM SUPPLY VOLTAGE	**0.9 V**	**0.8 V**	**0.7 V**	**0.6 V**	**0.5 V**
MAXIMUM POWER DISSIPATION	**150 W**	**190 W**	**200 W**	**200 W**	**200 W**
MAXIMUM NUMBER OF I/O PINS	3000	4000	4000	5300	7000


Processor Supply Voltage
Power Supply (Volt)
100
10
1
1970
1980
1990
2000
2010

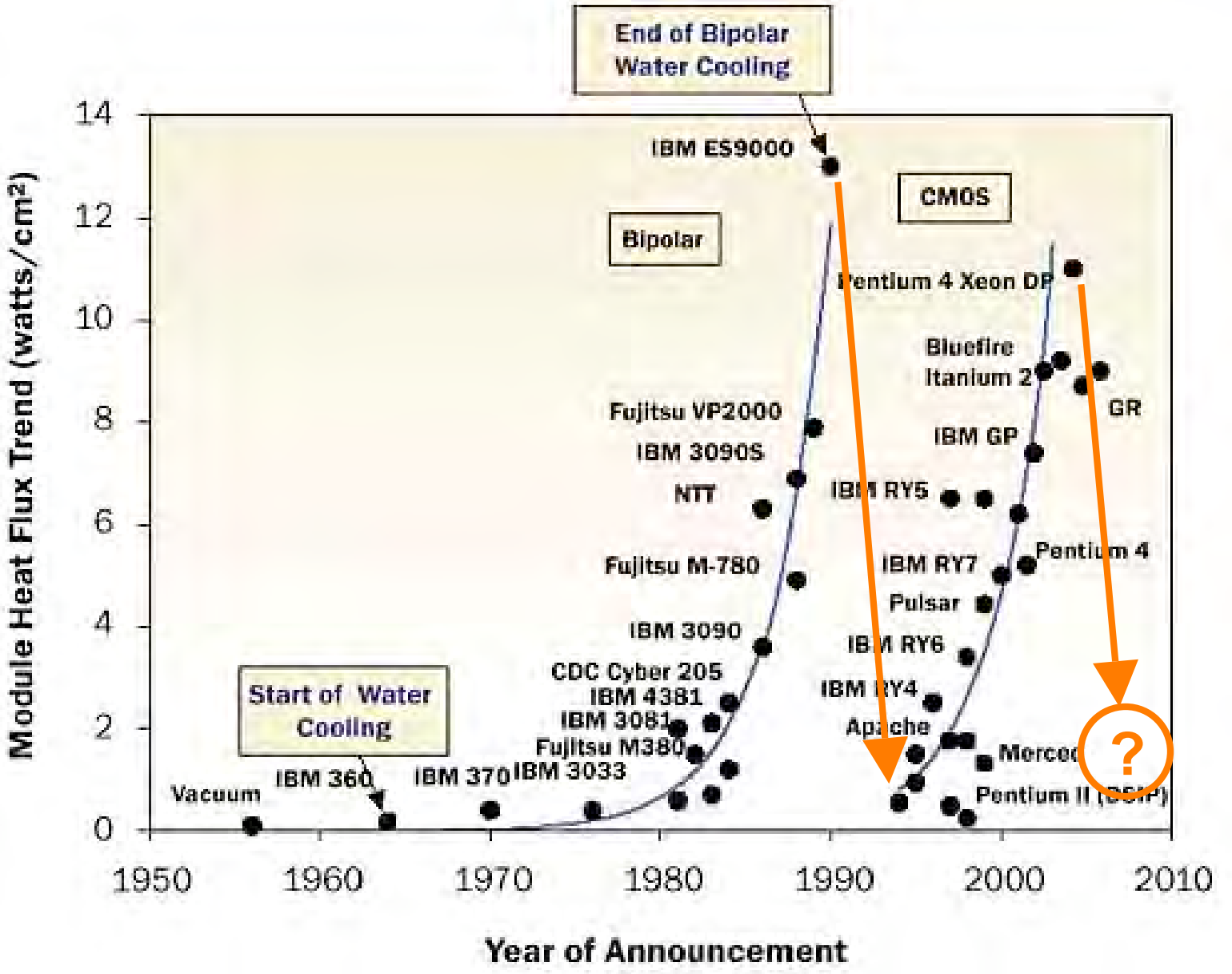

Voltage
Power
Current
Voltage [V]
Power per chip [W]
VDD current [A]
2.5
2
1.5
1
0.5
0
200
500
0
0
1998
2002
2006
2010
2014
Year

Temperature Map of IBM Power 4

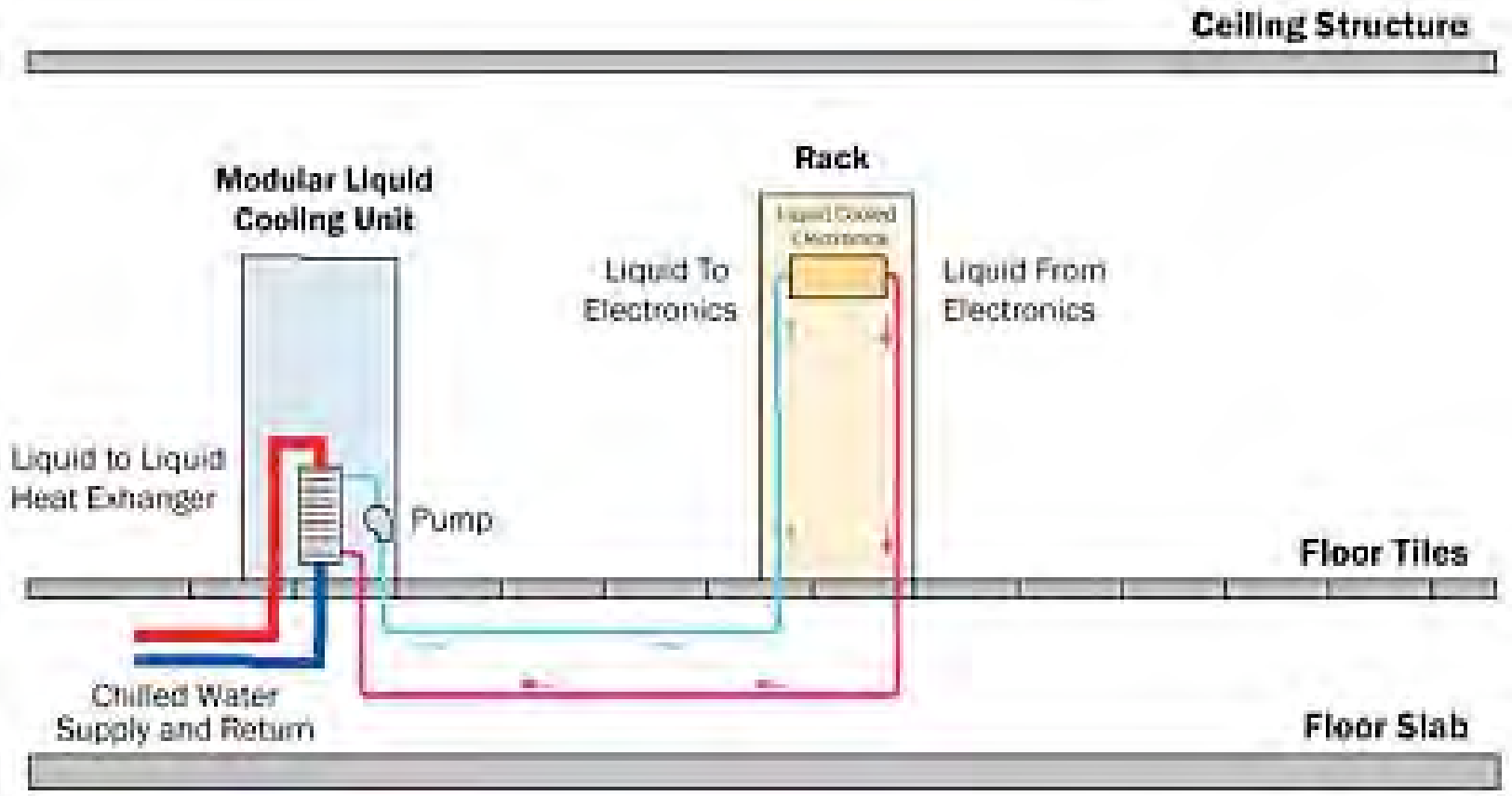
1.5 GHz Itanium-2



Courtesy of Intel Corporation and Prof. V. Oklobdzija (UC Davis)


End of Bipolar Water Cooling
IBM ES9000
CMOS
Bipolar
Pentium 4 Xeon DP
Bluefire
Itanium 2
GR
Fujitsu VP2000
IBM 3090S
IBM GP
NTT
IBM RY5
Fujitsu M-780
IBM RY7
Pentium 4
Pulsar
IBM 3090
IBM RY6
CDC Cyber 205
IBM 4381
IBM 3081
Fujitsu M380
IBM 3033
Start of Water Cooling
IBM 360
IBM 370
Vacuum
Apache
Pentium II
?
Module Heat Flux Trend (watts/cm²)
0
2
4
6
8
10
12
14
1950
1960
1970
1980
1990
2000
2010
Year of Announcement

Liquid Cooling Making A Comeback ?



CRAY

A Few Numbers About Power Density

- Goal: 1024 bit factorization.

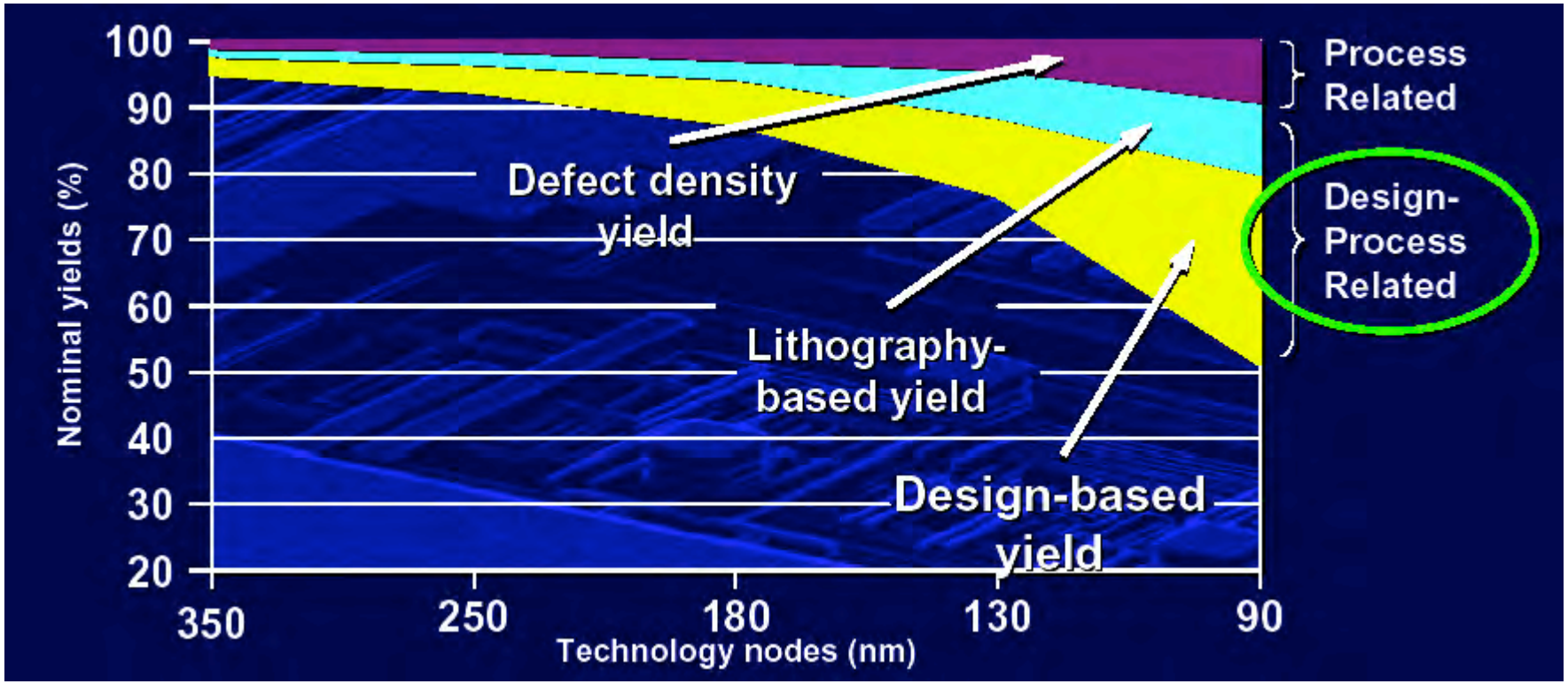
- Assume that we are building a system that consists of (300 x 90) = 27,000 ASIC chips, each measuring 1 cm^2, and operating at a clock frequency of 1 GHz.
- Required I/O bandwidth: 1024 Gb/s per chip
- The minimum power budget for high-speed communication: 5 mW/Gb/s
- Completely neglecting the logic+memory dissipation, only the power needed for communication is: 27,000 x 5 W = **135 kW**

A Few Numbers About Power Density

- Now assume that the 27,000 ASIC chips have a thickness of 1 mm each, and they are arranged (stacked) as closely to each other as possible.
- This results in a total volume of 0.0027 m^3
- Corresponding to a cube with 14 cm on each side.
- Longest space-diagonal distance (assuming direct path) is 30 cm, which is needed to sustain a clock speed of 1 GHz (ideal conditions: signal propagation length 30 cm in 1 ns).
- The power density of this cube will be **50 MW/m^3** !!

Yield Problems

Circuit Yield Becoming a Serious Problem !



Yield in Large Chips

Chip	Metal layers	Line width	Wafer cost	Def./ cm^2	Area mm^2	Dies/ wafer	Yield	Die cost
386DX	2	0.90	$900	1.0	43	360	71%	$4
486 DX2	3	0.80	$1200	1.0	81	181	54%	$12
Power PC 601	4	0.80	$1700	1.3	121	115	28%	$53
HP PA 7100	3	0.80	$1300	1.0	196	66	27%	$73
DEC Alpha	3	0.70	$1500	1.2	234	53	19%	$149
Super Sparc	3	0.70	$1700	1.6	256	48	13%	$272
Pentium	3	0.80	$1500	1.5	296	40	9%	$417

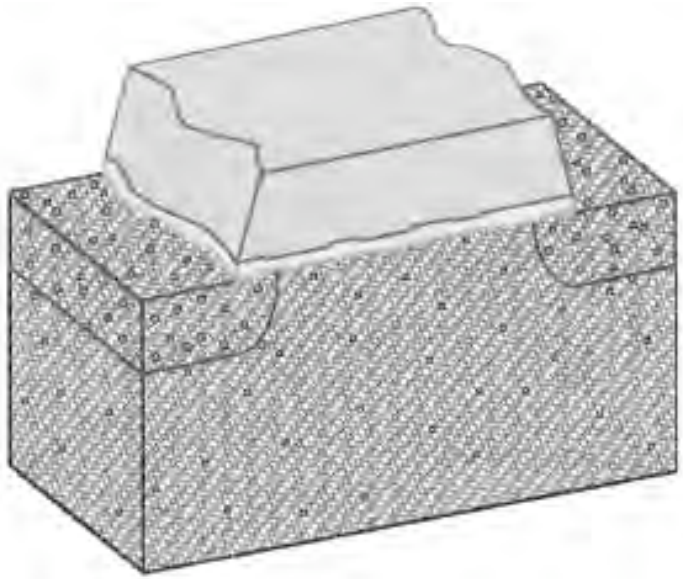
yield dropping with increasing die size

The problem is expected to become much more severe for nano-scale device technologies and novel devices.

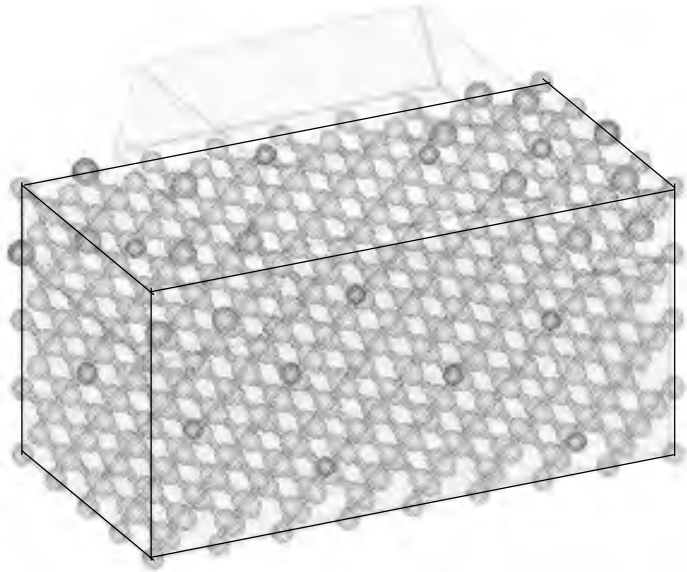
IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 50, NO. 9, SEPTEMBER 2003

Simulation of Intrinsic Parameter Fluctuations in Decananometer and Nanometer-Scale MOSFETs

Asen Asenov, *Member, IEEE* , Andrew R. Brown, John H. Davies, Savas Kaya, and Gabriela Slavcheva

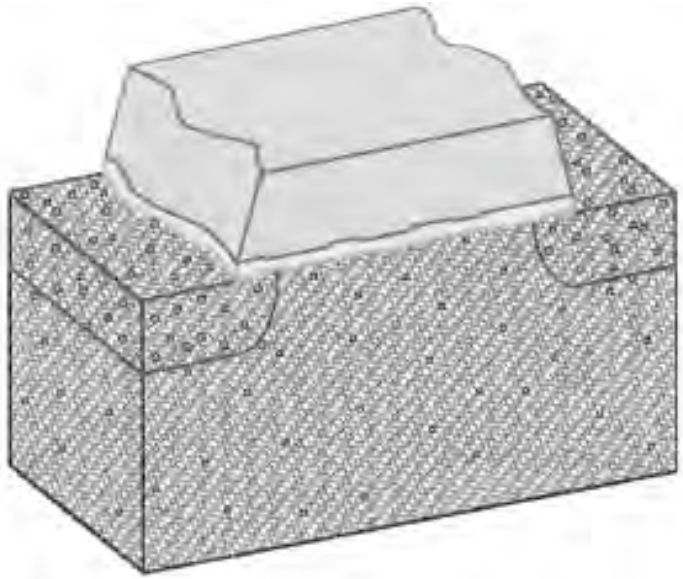


20 nm MOSFET (2010 ?)
50 Si atoms along the channel

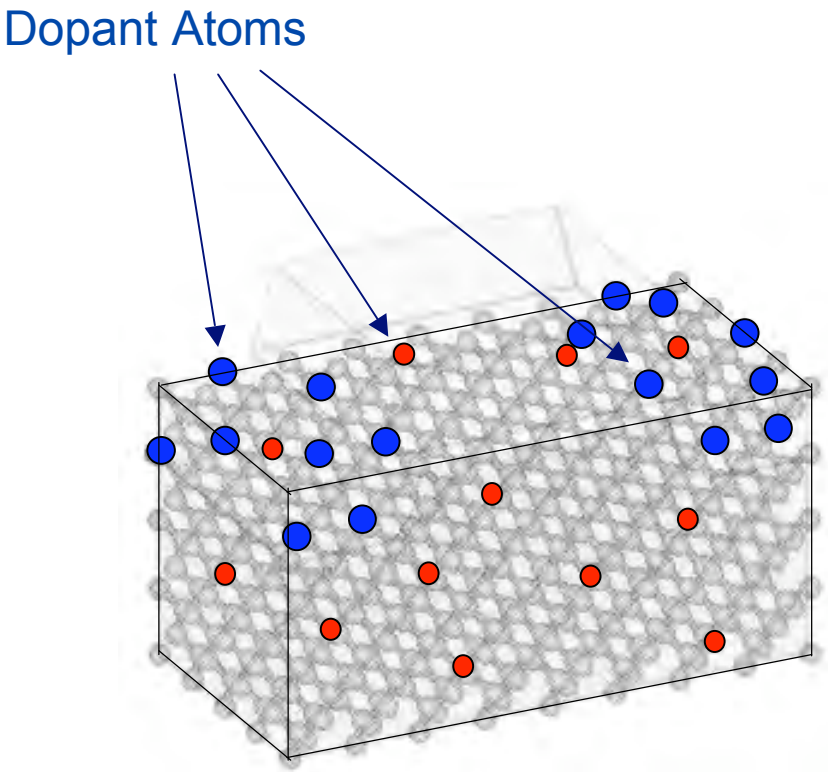


4 nm MOSFET (2020 ?)
10 Si atoms along the channel

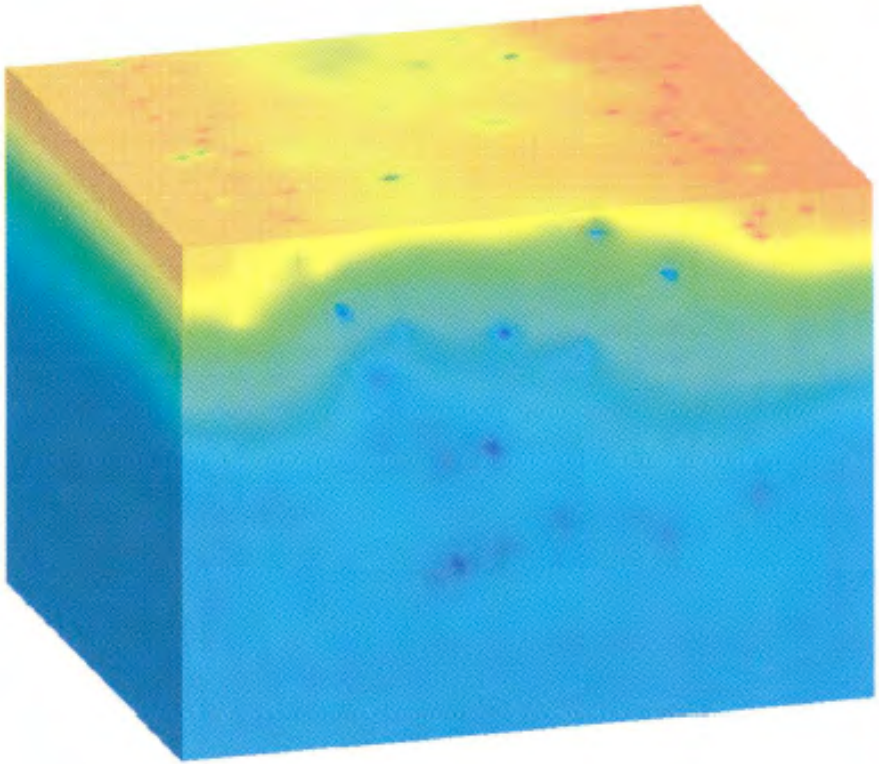
Strongly Irregular Device Behavior Expected !



20 nm MOSFET (2010 ?)
50 Si atoms along the channel

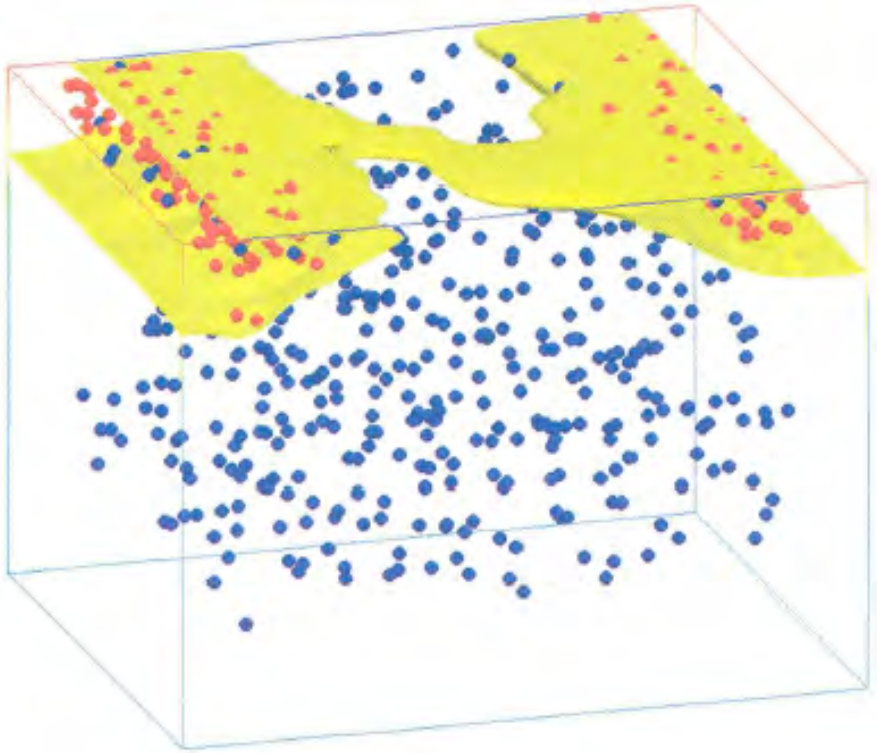


4 nm MOSFET (2020 ?)
10 Si atoms along the channel

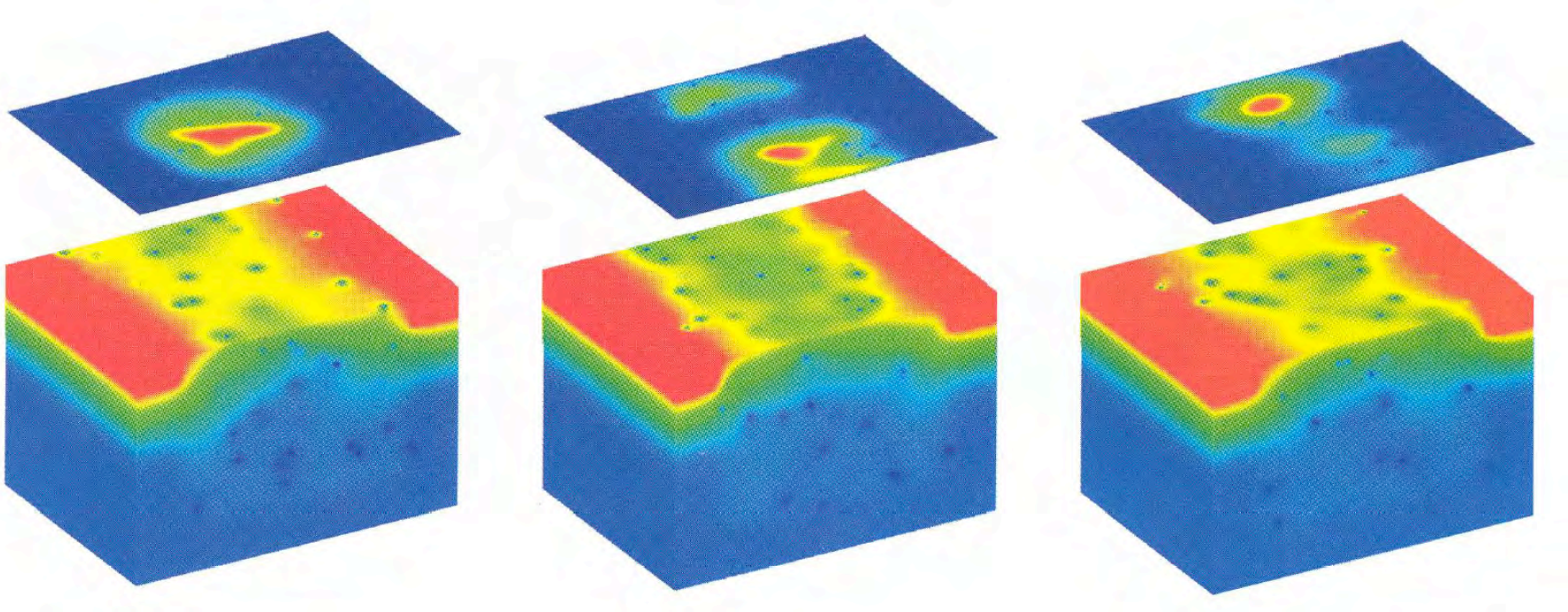


Potential distribution

Electron concentration profile
at channel inversion (turn-on)



50 nm x 50 nm MOSFET simulations



V_T = 0.49 V V_T = 0.65 V V_T = 0.85 V

Three different potential distributions and corresponding channel current fluctuations with random dopant atom positions

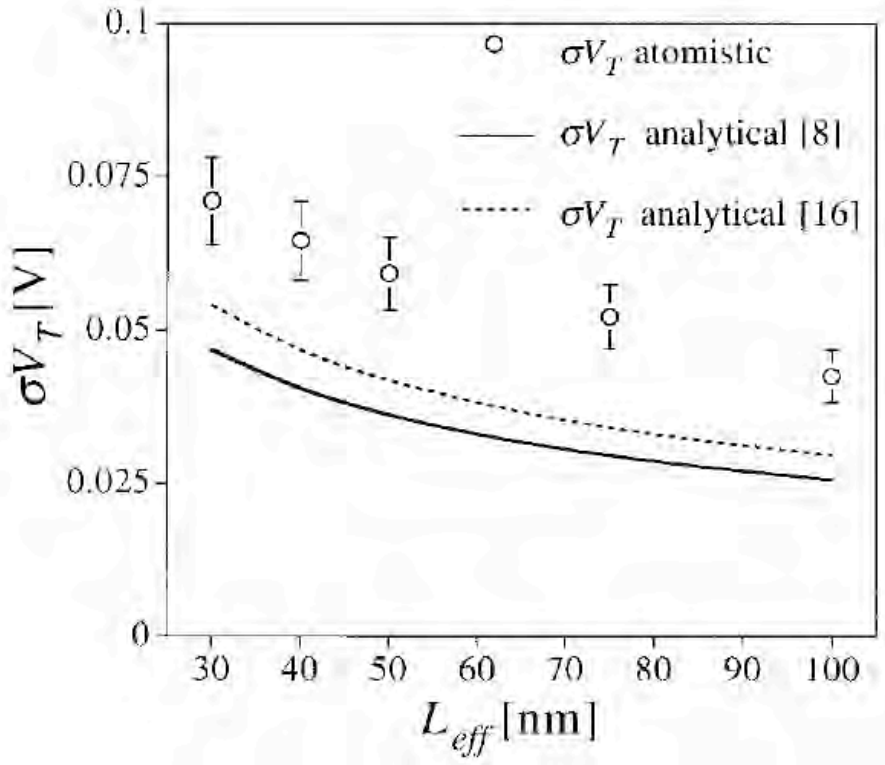
50 nm x 50 nm MOSFET simulations

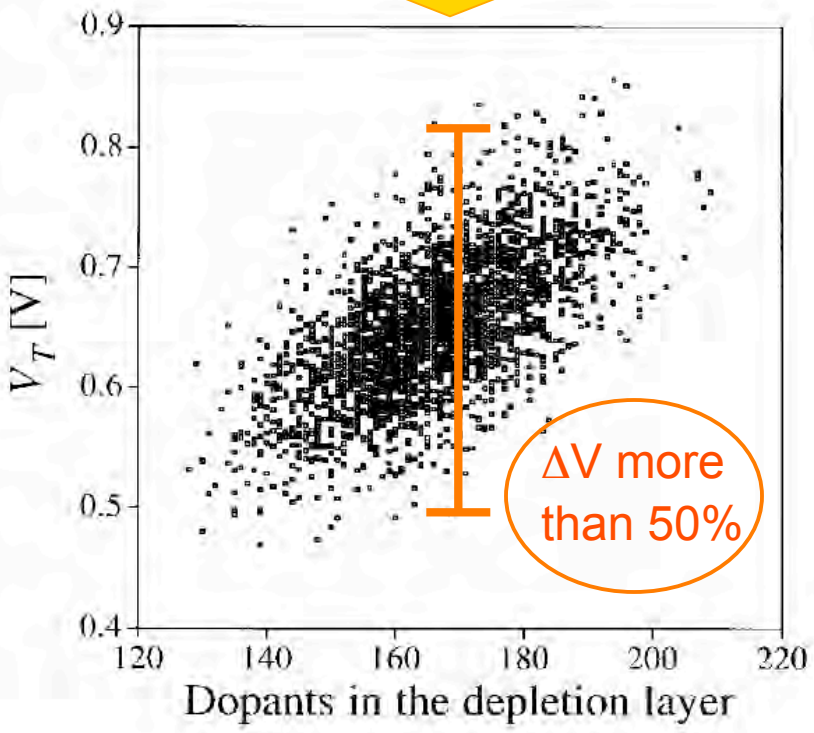
IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 45, NO. 12, DECEMBER 1998

Random Dopant Induced Threshold Voltage Lowering and Fluctuations in Sub-0.1 μm MOSFET's: A 3-D "Atomistic" Simulation Study

Asen Asenov

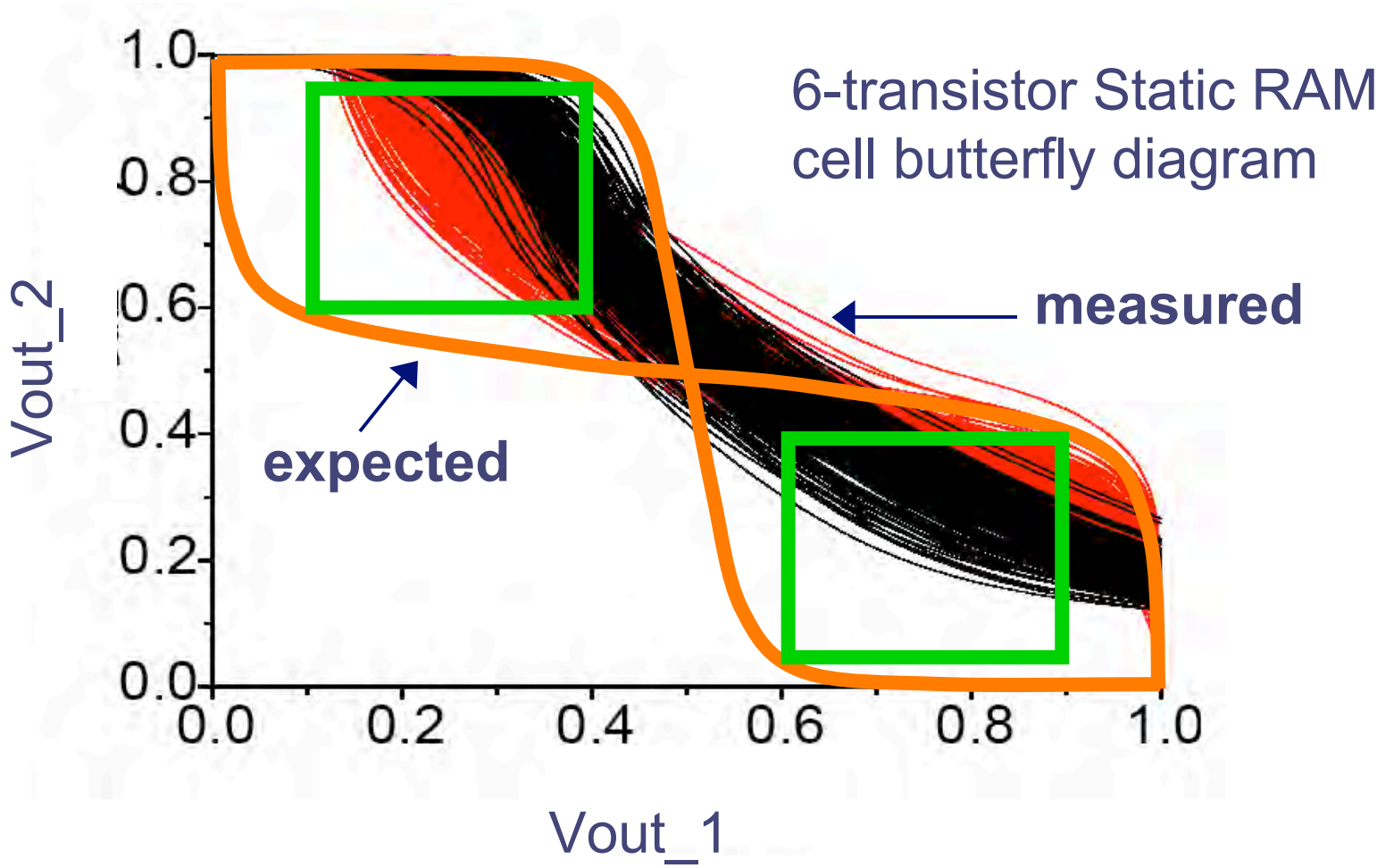
Dramatic fluctuation of the threshold voltage even with the same number of dopant atoms !





170 dopant atoms in the channel

Influence of Parameter Variations



The Future of CMOS and Nanotechnologies

Table 59a Single-gate Non-classical CMOS Technologies

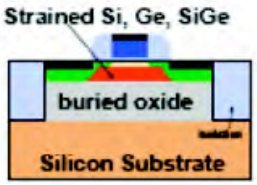
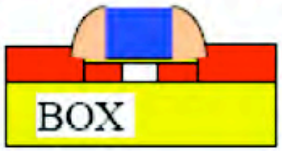
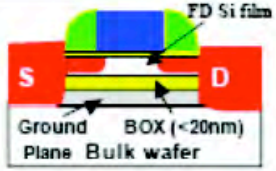
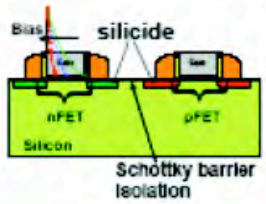
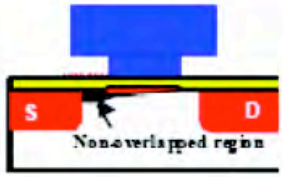
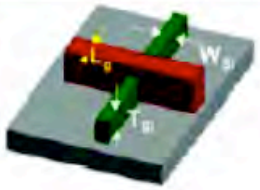
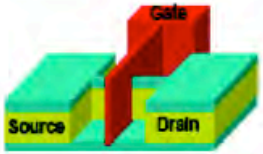
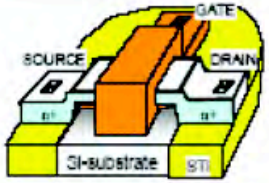
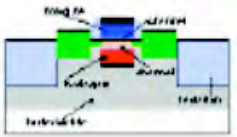
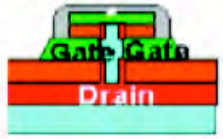
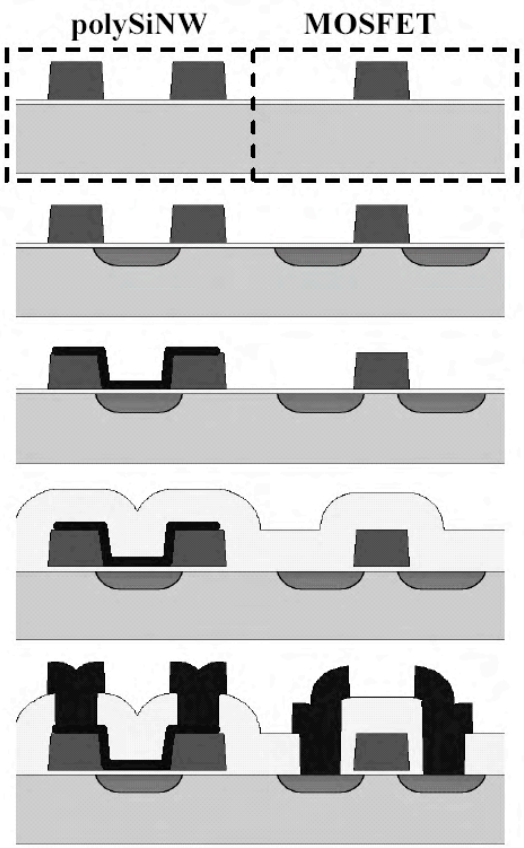
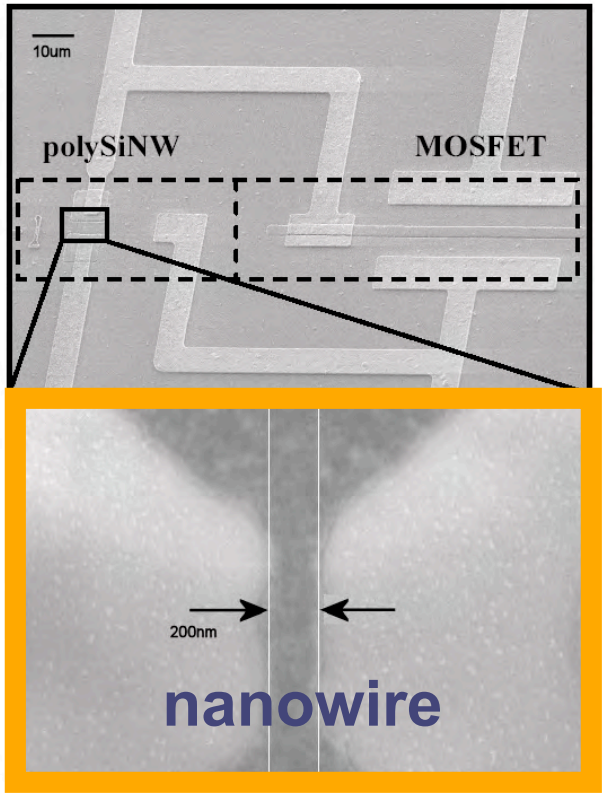
Transport-enhanced FETs	*Ultra-thin Body SOI FETs*		*Source/Drain Engineered FETs*	
				

Table 59b Multiple-gate Non-classical CMOS Technologies

Multiple Gate FETs				
N-Gate (N>2) FETs	*Double-gate FETs*			
				

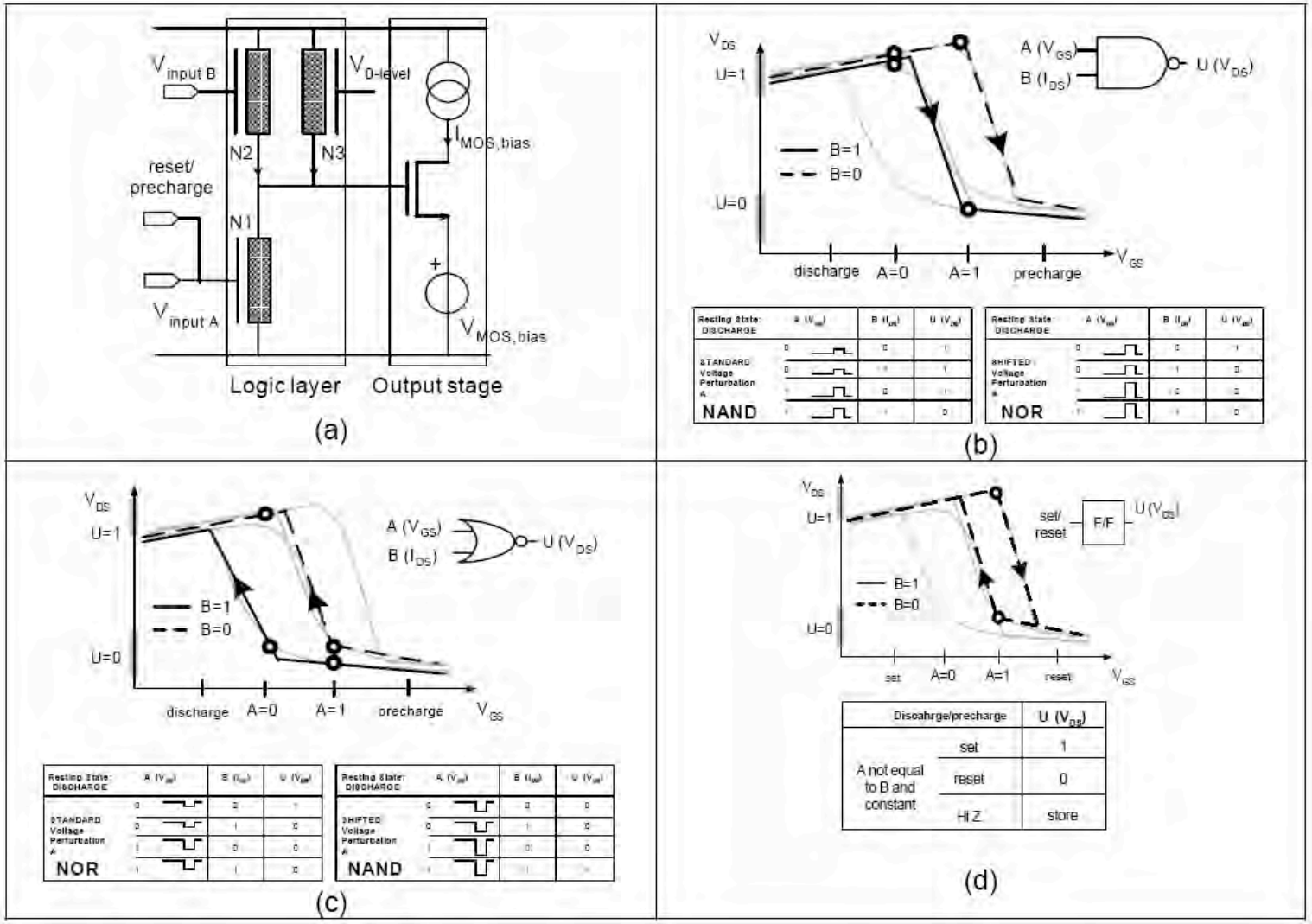
Novel Nanoelectronic Devices and Circuits

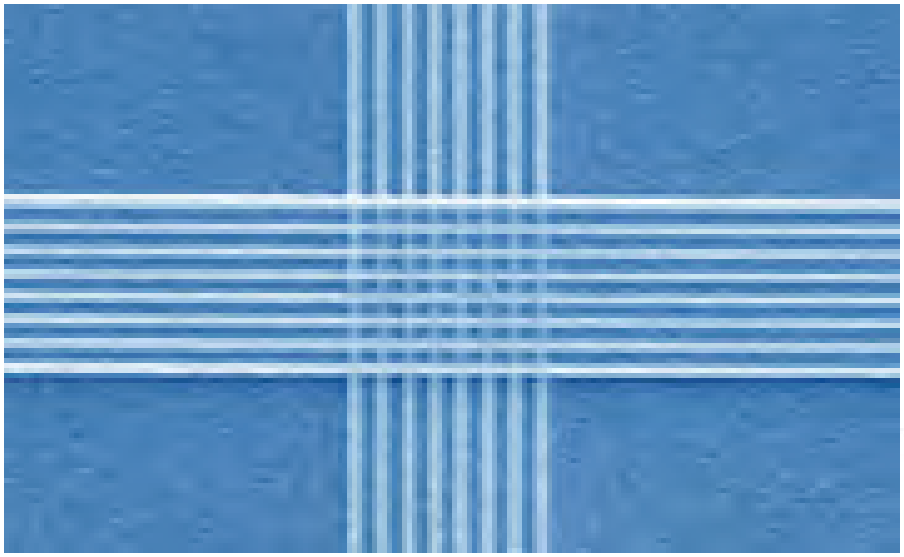


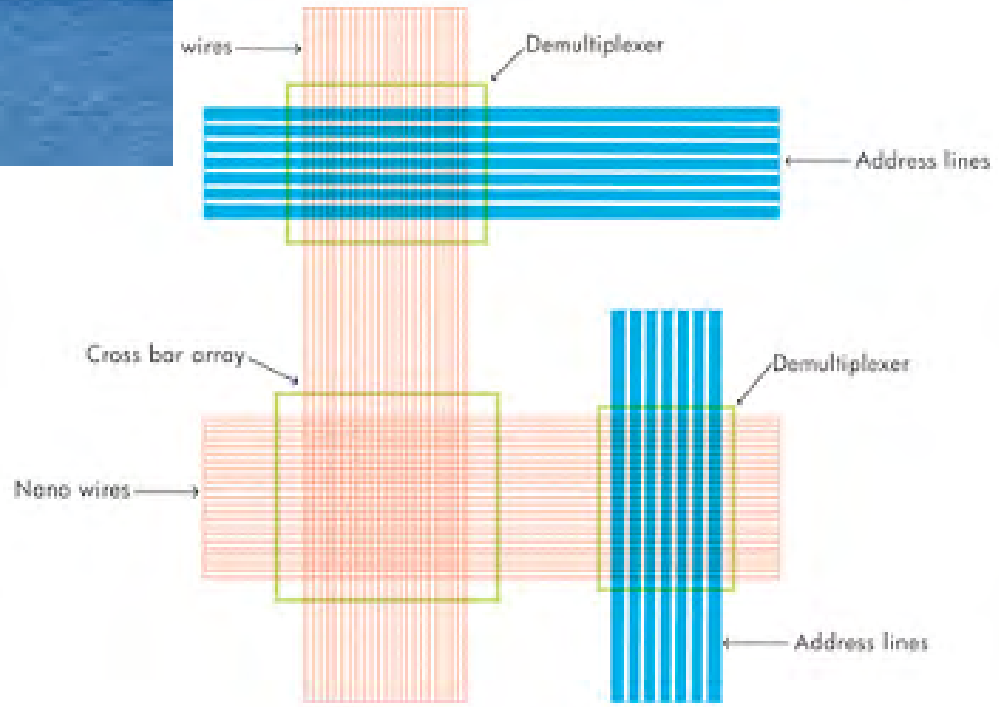


PolySi nanowire integrated with CMOS

Novel Nanoelectronic Devices and Circuits

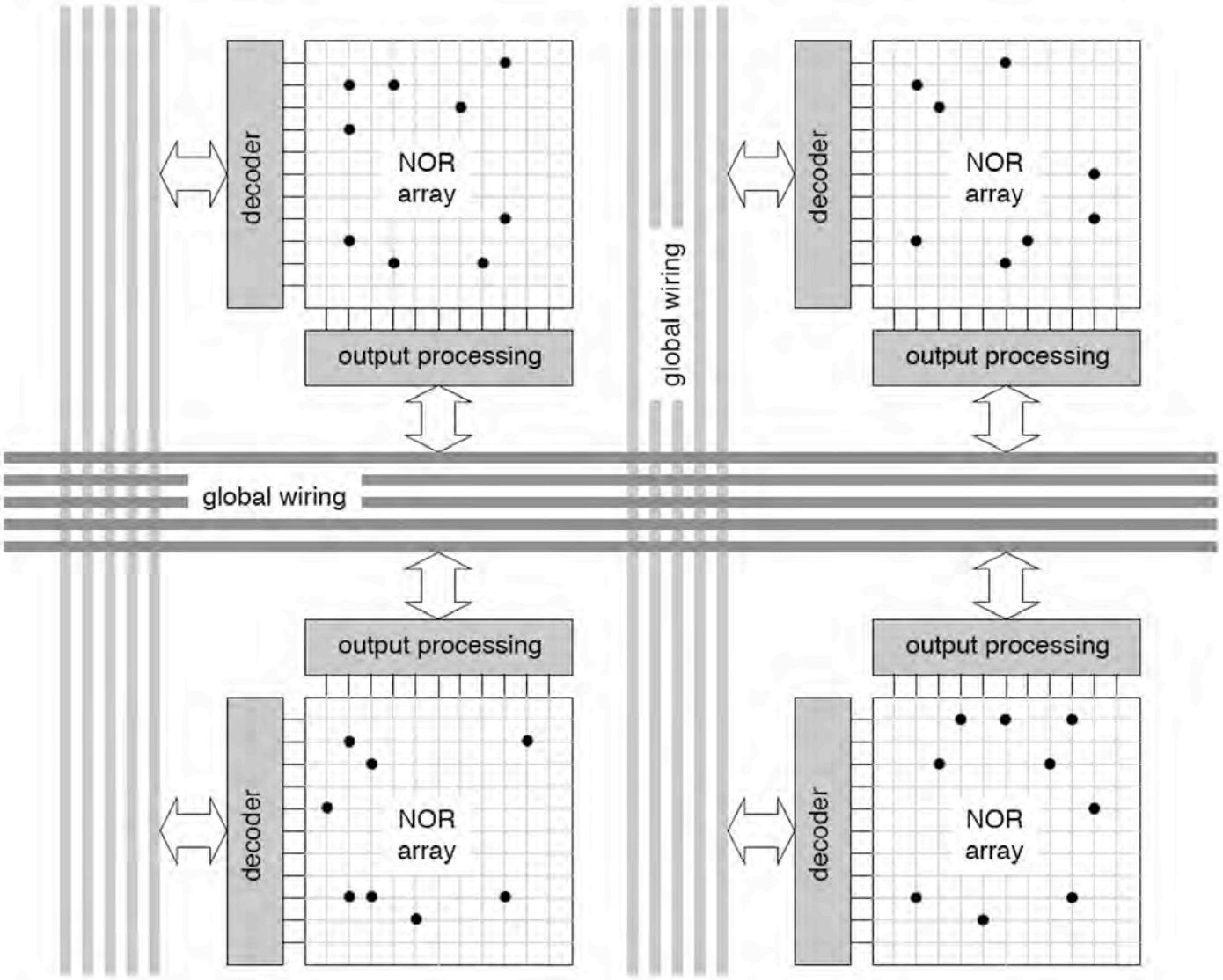


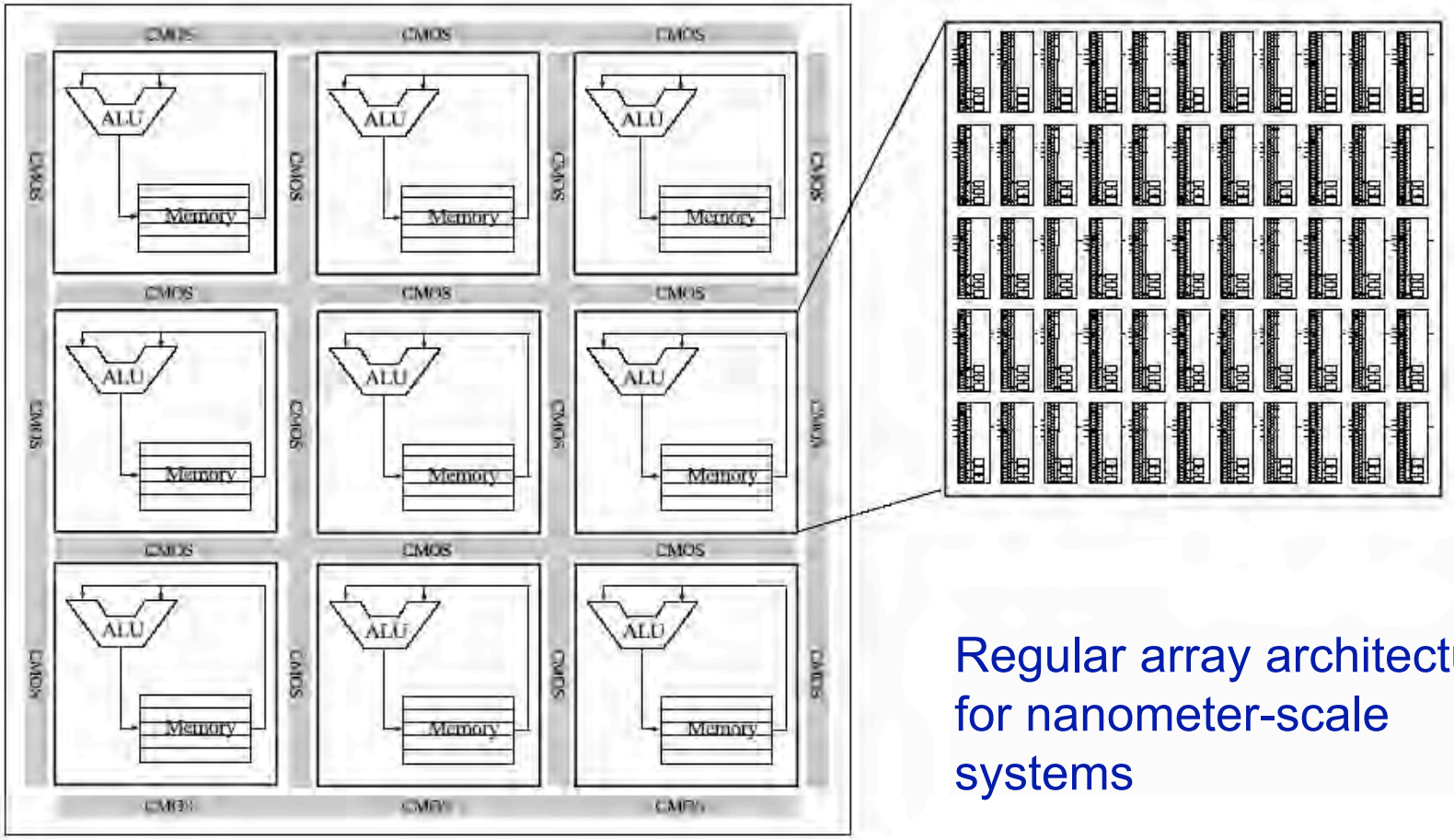




8 x 8 crossbar switch built with 40nm nanowires

HP Labs – 2005


decoder
NOR
array
output processing
global wiring
decoder
NOR
array
output processing
global wiring
output processing
decoder
NOR
array
output processing
decoder
NOR
array



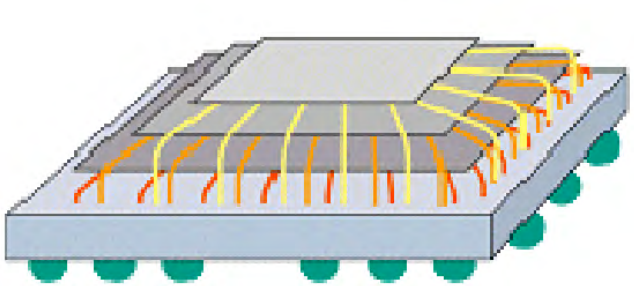
Regular array architecture for nanometer-scale systems

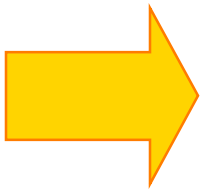
After David Lilja et al. (University of Minnesota)

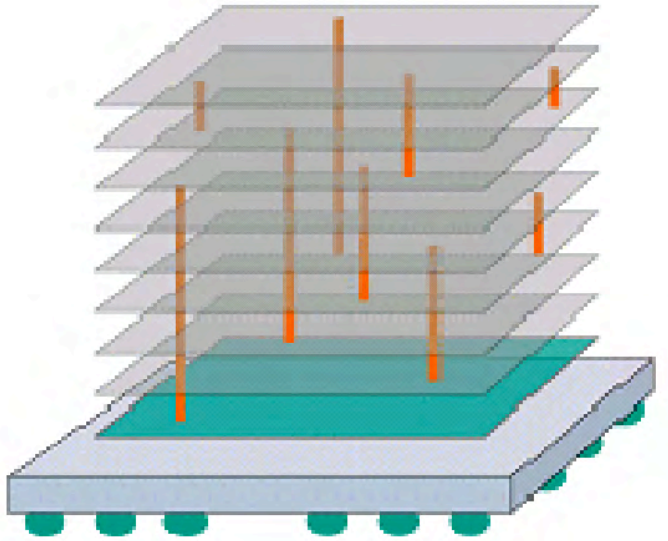
Stacking Multiple Chips

3D Integration ?

3D Integration ?



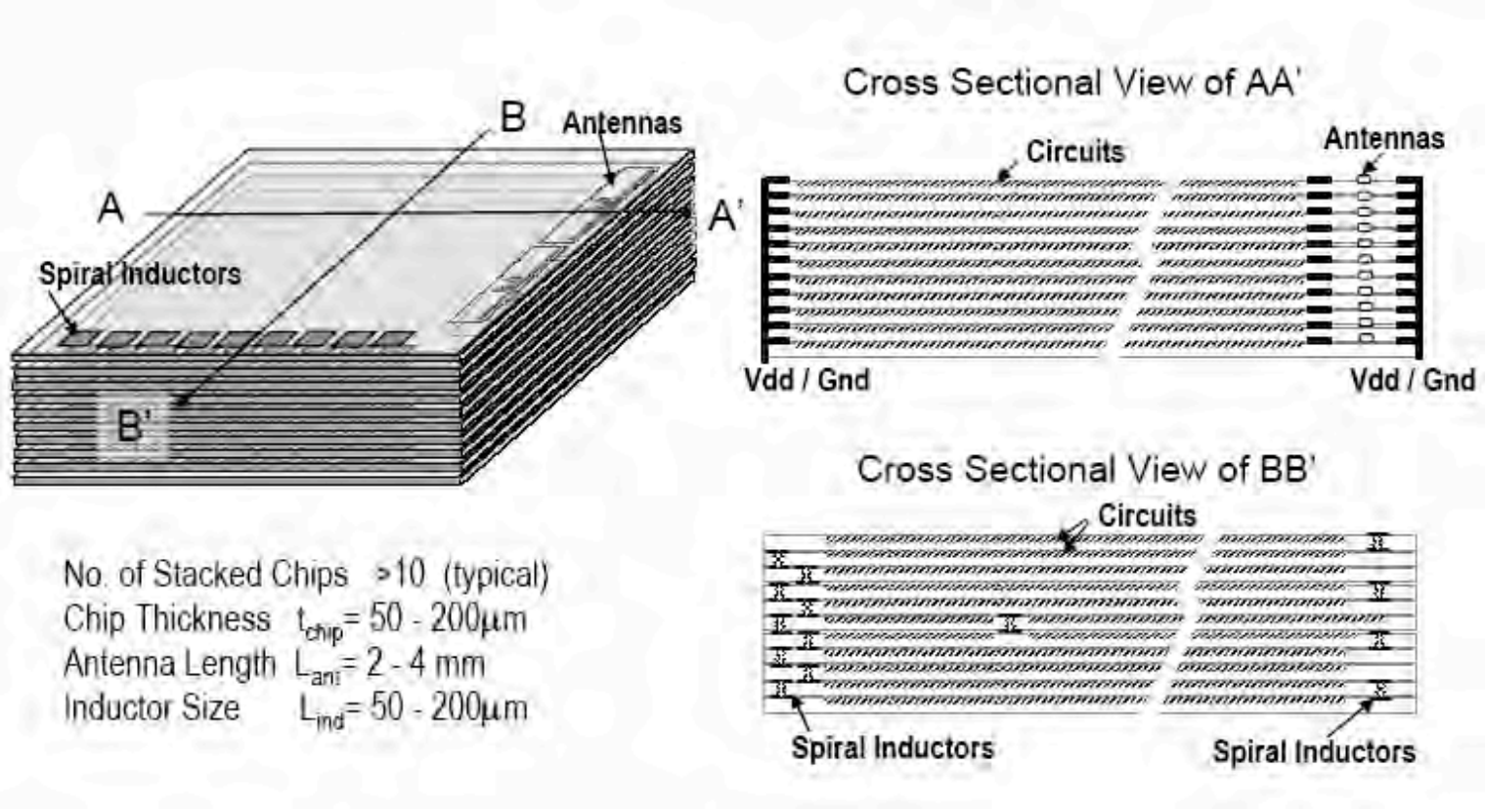




Wire-bonding multiple layers

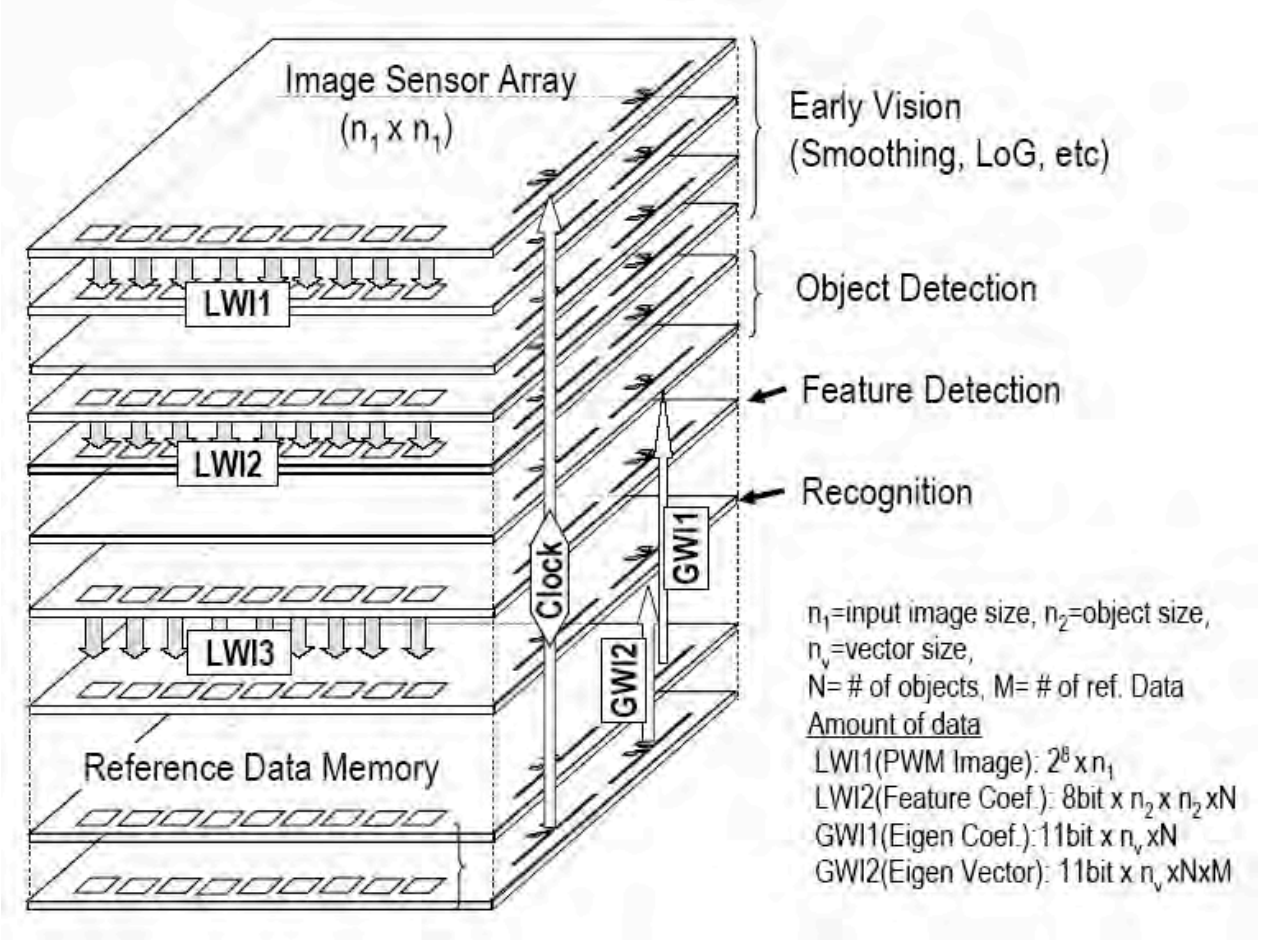
Direct stacking with integrated vertical links

Future Perspectives: 3D Integration (?)

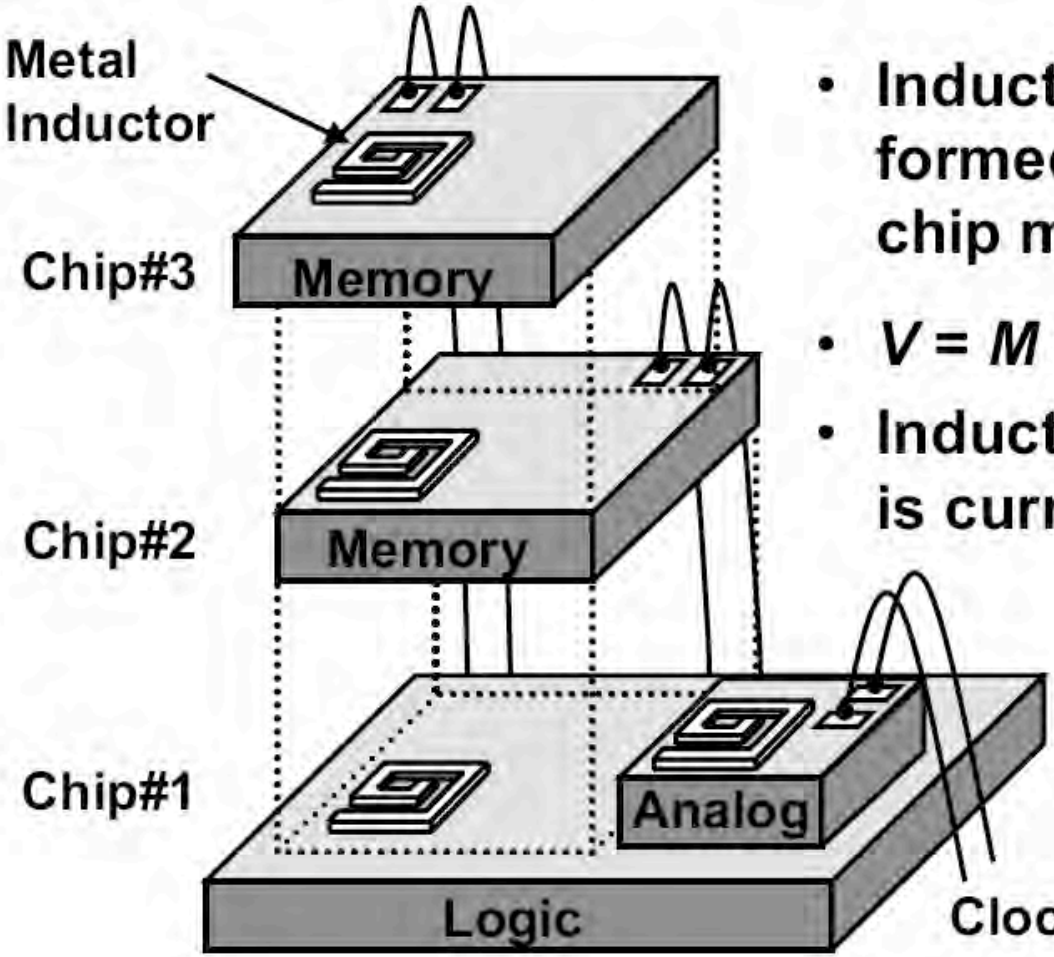


No. of Stacked Chips >10 (typical)
Chip Thickness t_{chip} = 50 - 200µm
Antenna Length L_{ant} = 2 - 4 mm
Inductor Size L_{ind} = 50 - 200µm

After Iwata et al., ISSCC 2005

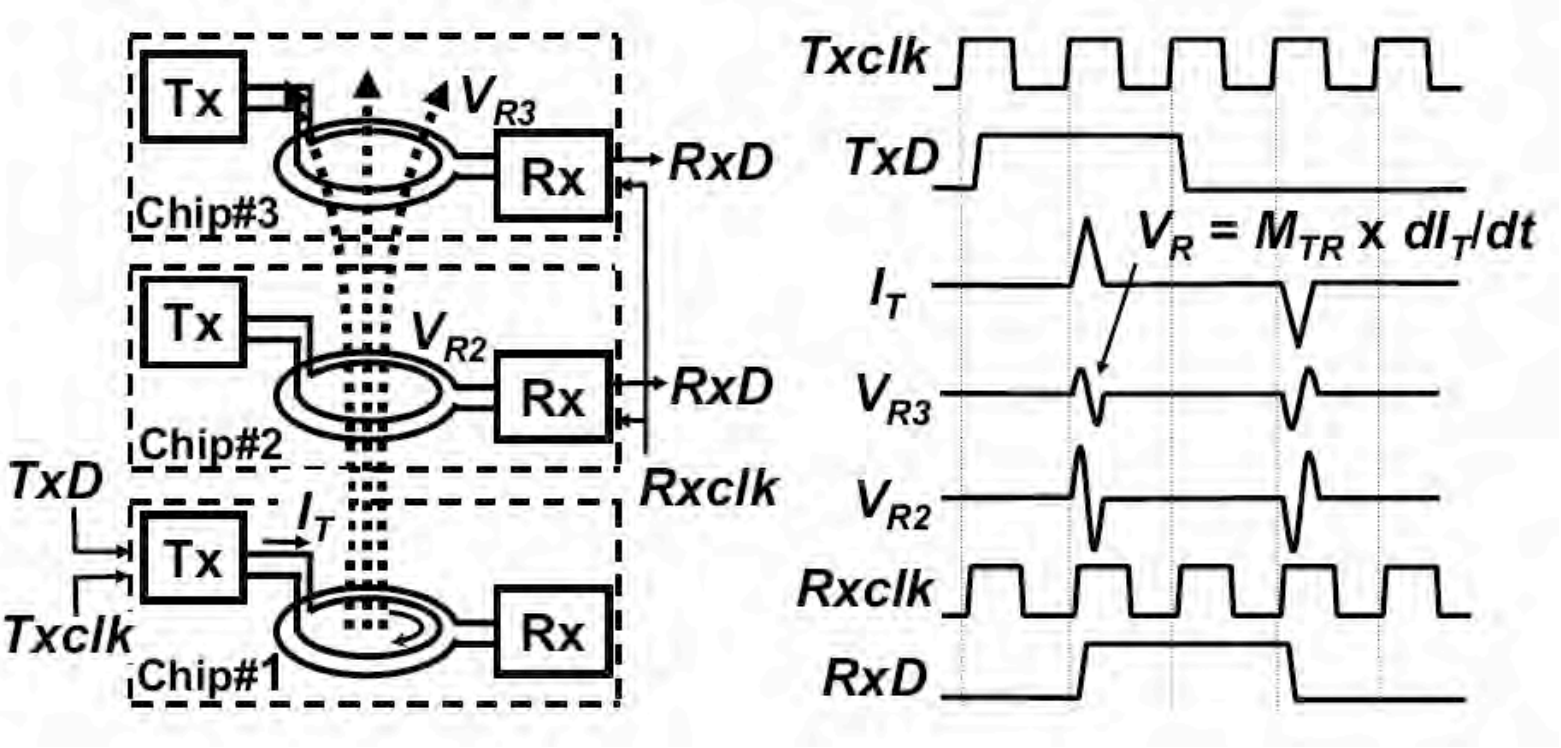


After Iwata et al., ISSCC 2005



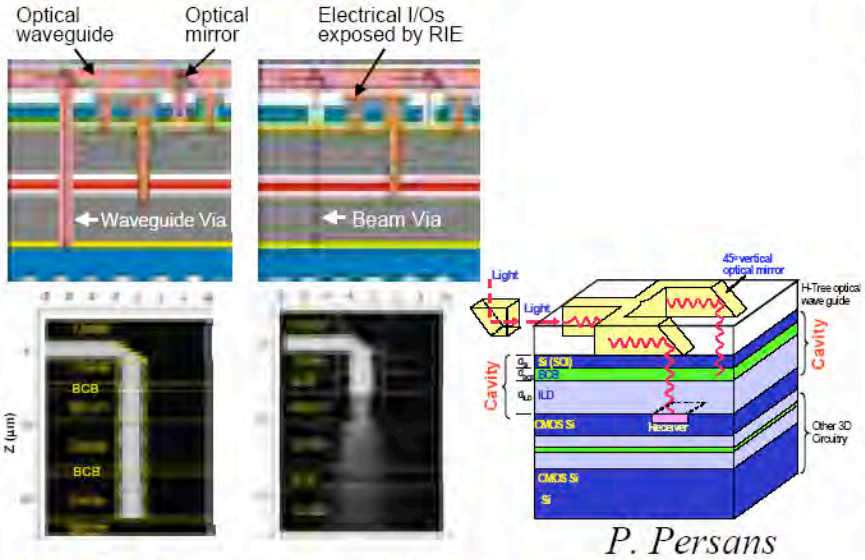
- Inductive coupling formed between on-chip metal inductors.
- $V = M\, dI/dt$
- Inductive coupling is current mode link.

After Mizoguchi et al, ISSCC 2004



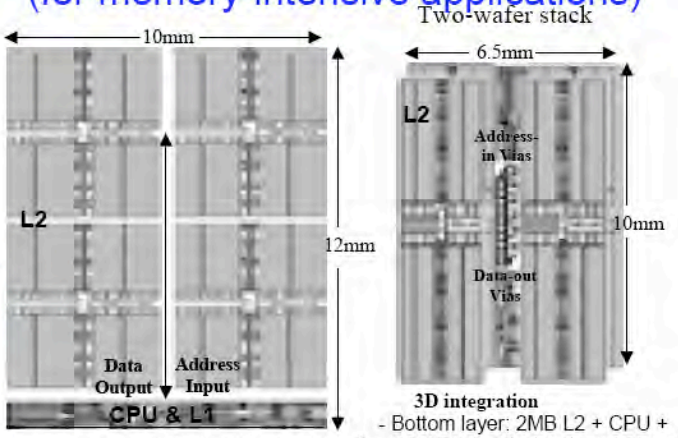
After Mizoguchi et al, ISSCC 2004

Optical Interconnects



P. Persans

Memory with Processor
(for memory-intensive applications)

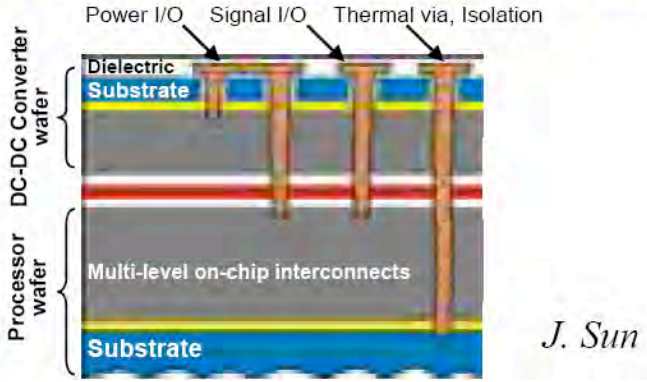


2D integration with die size of 120mm^2 (110mm^2 4MB L2 cache, 7mm^2 CPU and 3mm^2 120kB L1 cache)

3D integration
- Bottom layer: 2MB L2 + CPU + 120kB L1 with die size of 65mm^2
- Top layer: 2MB L2 with die size of 55mm^2 plus I/Os.

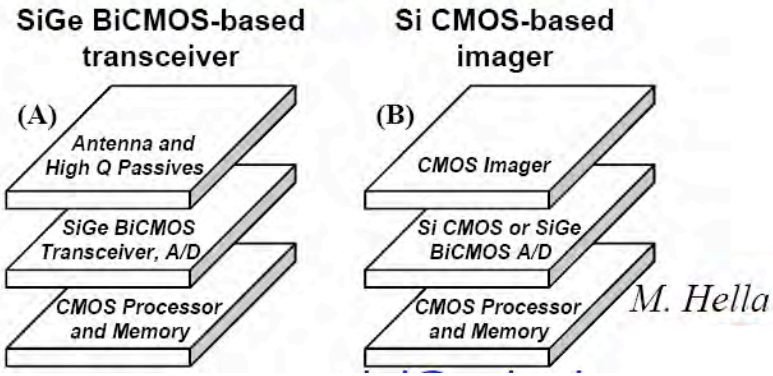
K. Rose

DC-DC Converter with Processor IC



J. Sun

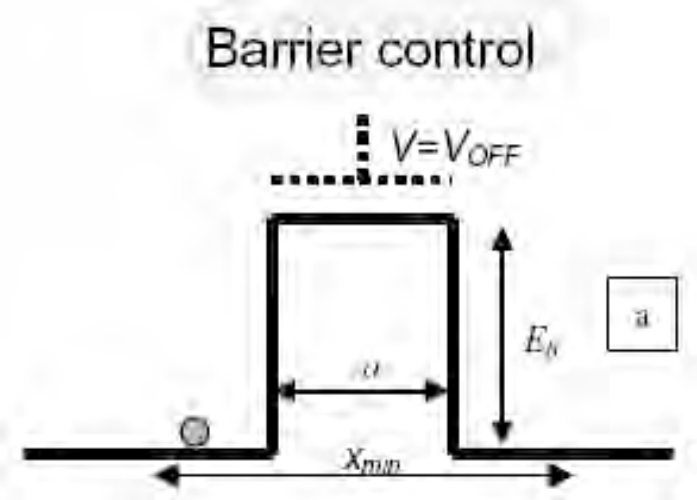
Smart-Wireless Applications



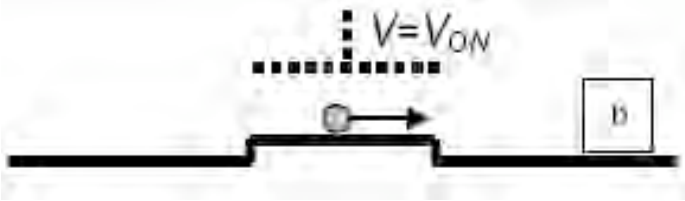
M. Hella

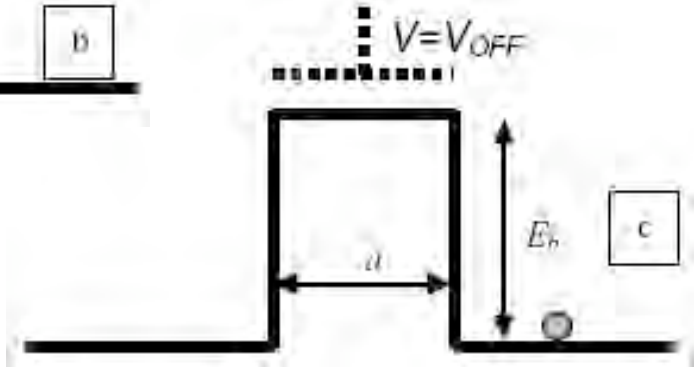
Fundamental Limits

Barrier Model of an Arbitrary Device



- Electrons are information carriers.
- Any electronic device used for information processing contains at least one energy barrier which controls electron position and flow.





After Cavin and Zhirnov, ESSDERC 2005

Fundamental Limits

- Shannon-von Neumann-Landauer (SNL) condition:

The minimum energy required for a binary transition = The minimum energy barrier height

$$E_{\text{bit}} \geq E_{\text{SNL}} = k_B T \ln 2 = 0.017 \text{ eV} \quad (T = 300 \text{ K})$$

- Heisenberg's uncertainty principle:

The minimum width of energy barrier to avoid spontaneous tunneling

$$a_{\min} \cong \frac{h}{\Delta p} = \frac{\hbar}{\sqrt{2 m_e E_b}} \approx 1.45 nm$$

Fundamental Limits

- Heisenberg's uncertainty principle again:

Minimum switching time

$$\tau_p = \frac{\pi\hbar}{\Delta E} = \frac{\pi\hbar}{k_B T \ln 2} \approx 0.11\,ps$$

- Information throughput B = Number of binary transitions per unit time

Power dissipation is proportional to information throughput

$$P = BE_{\text{bit}}$$

After Zhirnov, Cavin, Hutchby and Bourianoff, IEEE Proceedings 2003

Fundamental Limits

- Now imagine a chip containing:

  Smallest possible binary switches,
  Packed to maximum possible density,
  Operating at highest possible frequency, and
  Operating at the lowest possible energy per bit

After Zhirnov, Cavin, Hutchby and Bourianoff, IEEE Proceedings 2003

Fundamental Limits

- Now imagine a chip containing:

  Smallest possible binary switches,
  Packed to maximum possible density,
  Operating at highest possible frequency, and
  Operating at the lowest possible energy per bit

- The **power density** will be:

$$P = \frac{3 \cdot 10^{-21} J}{(1.45nm)^2 \cdot 0.11 ps} \approx 1.2 \cdot 10^6 \frac{W}{cm^2}$$

After Zhirnov, Cavin, Hutchby and Bourianoff, IEEE Proceedings 2003

Some Closing Observations

- Classical CMOS technology appears to be nearing its limits.
- Alternatives exist, but none of them a clear winner.
- Smaller devices and higher (local) speed does not appear to be a problem in the near future.
- Then again, we are within one order of magnitude of the fundamental limits for size and switching speed.
- Above all, **power dissipation** / **power density** seems to limit the performance of future devices and systems.